EIC NPL SEARCH
10/601,136 9/24/07 TLM

```
Set     Items   Description
S1       7017   INSTRUCTION?(2N)DECOD?
S2         16   S1(2N)(PREFIX? OR PRE()FIX???)
S3        491   S1:S2(3N)(DEDICAT? OR SEPARATE? OR SINGULAR? OR UNIQUE?
OR
              LONE? OR UNIQUE OR RESPECT? OR INDIVIDUAL? OR SPECIF? OR
PART-
              ICUL?)
S4        953   SHIFT?(2N)PREFIX?(2N)INSTRUCT? OR SHIFT?(2W)INSTRUCT?
S5    5678417   RULES? OR TERM? ? OR CONDITION? OR OPTION? OR DIRECT?
OR P-
              ROCEDURE?
S6     100476   S5(5N)(STORE? ? OR STORING OR SAVE? ? OR ACCUMULAT?
CACHE?
              OR CACHING OR STOCK? OR SAVING OR KEEP???)
S7      28561   (DEDICAT? OR SEPARATE? OR SINGULAR? OR UNIQUE? OR LONE?
OR
              UNIQUE OR RESPECT? OR INDIVIDUAL? OR SPECIF? OR
PARTICUL?)(2W-
              )(REGISTER? OR RAM OR DATABASE? OR BUFFER? OR QUEUE?)
S8         91   (ONLY OR SOLELY OR EXCLUSIV? OR JUST OR SIMPLY OR
PARTICUL-
              ARLY OR PRIMARILY OR EXACTLY OR PRECISELY OR
NOTHING()BUT)(3N-
              )(PREFIX? OR PRE()FIX??? OR PREFIX?(2N)(COMMAND? OR S5))
S9          8   S8(5N)(DECOD??? OR RE()ORDER??? OR RECONFIG? OR
REFORMULAT?
               OR RESET? OR SELECT? OR RE()SELECT? OR DECIPHER? OR
DECRYPT?)
S10        50   S3:S4 AND S5 AND S7
S11         0   S10 AND S9
S12       313   (DECOD??? OR RE()ORDER??? OR RECONFIG? OR REFORMULAT?
OR R-
              ESET? OR SELECT? OR RE()SELECT? OR DECIPHER? OR
DECRYPT?)(3N)-
              (PREFIX? OR PRE()FIX??? OR PREFIX?(2N)(COMMAND? OR S5))
S13         1   S10 AND S12
S14         8   S3:S4 AND (S8 OR S12)
S15         0   S3:S4 AND S9
S16        12   S3:S4 AND S6 AND S7
S17    198865   (DECOD??? OR RE()ORDER??? OR RECONFIG? OR REFORMULAT?
OR R-
              ESET? OR SELECT? OR RE()SELECT? OR DECIPHER? OR
DECRYPT?)(5N)-
              (INSTRUCTION? OR COMMAND? OR S5)
S18     10216   S17(5N)(CHANG??? OR ADAPT? OR ALTER? OR REARRANG? OR
MODIF?
               OR REVIS? ? OR EDIT???)
S19        19   S18 AND S6 AND S7
S20         3   (S2:S3 OR S4) AND S19
S21        11   S16 NOT S13:S14
S22         2   S20 NOT S13:S14
S23        11   S21:S22
S24       674   (CHECK? OR ANALY? OR DETECT? OR ASSESS? OR DETERMIN? OR
EX-
              AMIN? OR JUDG??? OR MONITOR? OR INSPECT?)(5N)(PREFIX? OR
PRE(-
```

```
             )FIX??? OR PREFIX?(2N)(COMMAND? OR S5))
S25           9   (S2:S3 OR S4) AND S24
S26          16   (S2:S3 OR S4) AND FETCH?(2N)CIRCUIT?
S27          24   S25:S26
S28          17   S27 NOT (S9 OR S13:S16 OR S20:S23)
S29          93   S4/TI
S30           3   S29 AND S3
S31           2   S29 AND S6 AND S7
S32          19   S13:S16 OR S20:S23
S33           5   S30:S31
S34           0   S28 AND S29
S35          17   S28 NOT S33
S36          17   S35 NOT S32:S33
File 350:Derwent WPIX 1963-2007/UD=200757
         (c) 2007 The Thomson Corporation
File 347:JAPIO Dec 1976-2007/Mar(Updated 070809)
         (c) 2007 JPO & JAPIO
```

13/69,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008443213 - Drawing available
WPI ACC NO: 1997-052545/199705
Microprocessor with expanded functionality within existing architecture -
has control unit detecting presence of segment override prefixes in instruction code sequences executed in flat memory mode and using prefix
value to control in- and or external functions
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI); ADVANCED MICRO DEVICES
LTD (ADMI)
Inventor: CHRISTIE D S; DUTTON D J
Patent Family (13 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1996041257	A1	19961219	WO 1996US9986	A	19960607	199705	B
US 5680578	A	19971021	US 1995479782	A	19950607	199748	E
EP 834118	A1	19980408	EP 1996923277	A	19960607	199818	E
			WO 1996US9986	A	19960607		
US 5768574	A	19980616	US 1995481704	A	19950607	199831	E
			US 1997914698	A	19970819		
US 5822778	A	19981013	US 1995474400	A	19950607	199848	E
			US 1997886421	A	19970701		
EP 834118	B1	19990331	EP 1996923277	A	19960607	199917	E
			WO 1996US9986	A	19960607		
DE 69601939	E	19990506	DE 69601939	A	19960607	199924	E
			EP 1996923277	A	19960607		
			WO 1996US9986	A	19960607		
ES 2129271	T3	19990601	EP 1996923277	A	19960607	199928	E
JP 11507453	W	19990629	WO 1996US9986	A	19960607	199936	E
			JP 1997502131	A	19960607		
KR 1999022430	A	19990325	WO 1996US9986	A	19960607	200023	E
			KR 1997708910	A	19971205		
CN 1187255	A	19980708	CN 1996194492	A	19960607	200336	E
			WO 1996US9986	A	19960607		
KR 448675	B	20041213	WO 1996US9986	A	19960607	200525	E
			KR 1997708910	A	19971205		
JP 3698441	B2	20050921	WO 1996US9986	A	19960607	200562	E
			JP 1997502131	A	19960607		

Priority Applications (no., kind, date): US 1997914698 A 19970819; US 1997886421 A 19970701; US 1995481704 A 19950607; US 1995479782 A 19950607; US 1995474400 A 19950607

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1996041257	A1	EN	28	6	

National Designated States,Original: CN JP KR
Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT
LU MC NL PT SE

US 5680578	A	EN	13	6	
EP 834118	A1	EN		0	PCT Application WO 1996US9986 Based on OPI patent WO 1996041257
Regional Designated States,Original: DE ES FR GB					
US 5768574	A	EN			Continuation of application US 1995481704
US 5822778	A	EN			Continuation of application US 1995474400
EP 834118	B1	EN			PCT Application WO 1996US9986 Based on OPI patent WO 1996041257
Regional Designated States,Original: DE ES FR GB					
DE 69601939	E	DE			Application EP 1996923277 PCT Application WO 1996US9986 Based on OPI patent EP 834118 Based on OPI patent WO 1996041257
ES 2129271	T3	ES			Application EP 1996923277 Based on OPI patent EP 834118
JP 11507453	W	JA	39		PCT Application WO 1996US9986 Based on OPI patent WO 1996041257
KR 1999022430	A	KO		6	PCT Application WO 1996US9986 Based on OPI patent WO 1996041257
CN 1187255	A	ZH			PCT Application WO 1996US9986 Based on OPI patent WO 1996041257
KR 448675	B	KO			PCT Application WO 1996US9986 Previously issued patent KR 99022430 Based on OPI patent WO 1996041257
JP 3698441	B2	JA	15		PCT Application WO 1996US9986 Previously issued patent JP 11507453 Based on OPI patent WO 1996041257

Alerting Abstract WO A1

The microprocessor includes an address translation unit (ATU) (116) generating a physical address from a logical one and a segment value. Several segment registers are coupled to the ATU, one storing the segment value. A control unit coupled to the ATU detects an instruction field indicative of one of the segment registers, and conveys a signal to the ATU indicative of it.

A confirmation register stores a value indicative of a microprocessor address translation mode. A second control unit coupled to the configuration register and the first control unit performs a function dependent on the stored value in the configuration register and on the signal from the first control unit.

ADVANTAGE - Code may be easily ported to processor implementing new functions, while overall nature of instruction set remains unchanged.

Title Terms/Index Terms/Additional Words: MICROPROCESSOR; EXPAND; FUNCTION;

EXIST; ARCHITECTURE; CONTROL; UNIT; DETECT; PRESENCE; SEGMENT; OVERRIDE;

INSTRUCTION; CODE; SEQUENCE; EXECUTE; FLAT; MEMORY; MODE; PREFIX; VALUE;

EXTERNAL

Class Codes
International Classification (Main): G06F-012/00, G06F-012/02, G06F-009/318
, G06F-009/32
US Classification, Issued: 395481000, 395479000, 395567000, 711206000, 711209000, 711208000, 395567000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03C
Original Titles:
...Microprocessor using an instruction field to expand the **condition** flags and a computer system employing the microprocessor...

Original Publication Data by Authority

Original Abstracts:
...to use the prefix value or the value stored in the associated segment
register to **selectively** enable **condition** flag modification for instructions. An instruction which modifies the **condition** flags and a **branch** instruction intended to branch based on the **condition** flags **set**
by the instruction may be separated by numerous instructions which do **not**
modify the **condition** flags. When the branch **instruction** is **decoded**
,
the **condition** flags it depends on **may** already be available. In another
embodiment of the **present** microprocessor, the segment register override
bytes are used to select between multiple sets of **condition** flags. Multiple **conditions** may be retained by the microprocessor for later examination. **Conditions** **which** a program **utilizes** multiple times in a
program may be maintained while **other** **conditions** may be generated and
utilized.

...

...Additional registers are available to a program other than the AMD.artwork. 80x86 Series architecture **specifies** , but the **instruction**
encoding is unchanged. Having more registers available to a program allows
for more operands to
Claims:
...plurality of segment registers to a control unit;operating said control
unit to select an **operand** register
?

14/69,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013927598 - Drawing available
WPI ACC NO: 2004-107513/200411
XRPX Acc No: N2004-085459
Instruction length decoding apparatus for complex instruction set computing architecture, has primary instruction length decoder that selects subset of instruction bytes, and decodes prefix **within subset of bytes**
Patent Assignee: MADDURI V R (MADD-I)
Inventor: MADDURI V R
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20030236964	A1	20031225	US 2002180389	A	20020625	200411 B

Priority Applications (no., kind, date): US 2002180389 A 20020625

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20030236964	A1	EN	10	5	

Alerting Abstract US A1
NOVELTY - An instruction streaming buffer (ISB) stores the instruction bytes. A primary instruction length decoder (ILD) stage selects a subset of instruction bytes, and **decodes** a **prefix** within instruction bytes. Secondary ILD stage decodes an instruction length of an instruction within the subset of instruction bytes, and aligns an instruction. Tertiary ILD stage calculates an actual instruction length of instruction based on the prefix.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

1.processor;

2.recorded medium storing instruction length decoding program;

3.instruction length decoding system; and

4.method for decoding instruction length.

USE - For processor (claimed) using complex instruction set computing (CISC) architecture, in computer system.
ADVANTAGE - Increases the rate of instruction output since the decoder speculatively decodes the instruction length. Improves instruction decoding performance by speculatively decoding the length of instruction in

parallel
manner.
DESCRIPTION OF DRAWINGS - The figure shows a flowchart explaining the instruction decoding process in the microprocessor.

Title Terms/Index Terms/Additional Words: INSTRUCTION; LENGTH; DECODE; APPARATUS; COMPLEX; SET; COMPUTATION; ARCHITECTURE; PRIMARY; SELECT; SUBSET; BYTE; PREFIX

Class Codes
International Classification (Main): G06F-009/30
US Classification, Issued: 712204000, 712209000, 712212000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03C; T01-M04

...**set computing architecture, has primary instruction length decoder that**
selects subset of instruction bytes, and decodes **prefix within subset**
of bytes
...bytes. A primary instruction length decoder (ILD) stage selects a
subset of instruction bytes, and **decodes** a **prefix** within instruction
bytes. Secondary ILD stage decodes an instruction length of an instruction
within the...

Original Publication Data by Authority

Claims:
...instruction length decoder (ILD) stage to select a subset of said instruction bytes, said first ILD stage comprising a **prefix decoder**
to **decode** a **prefix** within said instruction bytes; a second ILD **stage**
to speculatively **decode** an **instruction** length of an instruction within
said subset of instruction bytes, said second ILD stage comprising a **shift**
unit **to** align an instruction; a third ILD stage to calculate an actual
instruction **length** of said **instruction** based at least partially upon
said prefix.

14/69,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010060157 - Drawing available
WPI ACC NO: 2000-365791/200031
XRPX Acc No: N2000-273694
Variable byte length instruction predecoding method for superscalar microprocessors, involves predecoding fixed number of instructions bytes
starting with instruction bytes identified by predecode pointer
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: AHMED S F; MILLER P K; ZURASKI G D
Patent Family (7 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 2000026769	A1	20000511	WO 1999US12961	A	19990609	200031	B
US 6260134	B1	20010710	US 1998184750	A	19981102	200141	E
EP 1131698	A1	20010912	EP 1999927380	A	19990609	200155	E
			WO 1999US12961	A	19990609		
KR 2001075672	A	20010809	KR 2001705482	A	20010430	200211	E
JP 2002529809	W	20020910	WO 1999US12961	A	19990609	200274	E
			JP 2000580084	A	19990609		
EP 1131698	B1	20030521	EP 1999927380	A	19990609	200341	E
			WO 1999US12961	A	19990609		
DE 69908175	E	20030626	DE 69908175	A	19990609	200350	E
			EP 1999927380	A	19990609		
			WO 1999US12961	A	19990609		

Priority Applications (no., kind, date): US 1998184750 A 19981102

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 2000026769	A1	EN	46	14	
National Designated States,Original: JP KR					
Regional Designated States,Original: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1131698	A1	EN			PCT Application WO 1999US12961
					Based on OPI patent WO 2000026769
Regional Designated States,Original: DE FR GB					
JP 2002529809	W	JA	72		PCT Application WO 1999US12961
					Based on OPI patent WO 2000026769
EP 1131698	B1	EN			PCT Application WO 1999US12961
					Based on OPI patent WO 2000026769
Regional Designated States,Original: DE FR GB					
DE 69908175	E	DE			Application EP 1999927380
					PCT Application WO 1999US12961
					Based on OPI patent EP 1131698
					Based on OPI patent WO 2000026769

Alerting Abstract WO A1
NOVELTY - The fixed number of instruction bytes starting with instruction
byte identified by predecode pointer, are predecoded. The pointer is incremented and again the corresponding instruction bytes are predecoded.

DESCRIPTION - An INDEPENDENT CLAIM is also included for predecoder.
USE - For precoding instruction bytes of variable byte length instructions to identify bytes of variable length instructions in super season microprocessor used in computer system.
ADVANTAGE - The performance of microprocessor is improved by limiting the length detection time, routing time and **shifting** time of **instruction** bytes. By utilizing the predecoded information from the predecode unit, the instruction alignment can be implemented with relatively small number of cascaded level of logic gates and pipeline stages thereby facilitates high frequencies of operation.
DESCRIPTION OF DRAWINGS - The figure shows block diagram of predecode unit.

Title Terms/Index Terms/Additional Words: VARIABLE; BYTE; LENGTH; INSTRUCTION; METHOD; MICROPROCESSOR; FIX; NUMBER; START; IDENTIFY; POINT

Class Codes
International Classification (Main): G06F-009/30, G06F-009/38
US Classification, Issued: 712210000, 712204000, 712213000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-D02; T01-F03A; T01-F03C; T01-M06C

Alerting Abstract ...The performance of microprocessor is improved by limiting the length detection time, routing time and **shifting** time of **instruction** bytes. By utilizing the predecoded information from the predecode unit, the instruction alignment can be...

Original Publication Data by Authority

Claims:
...a set of possible prefix byte values;a prefix accumulator circuit (310) coupled to said **decode** circuit and said **prefix** find circuit and configured to output a plurality of position length vectors each corresponding to one of **said** fixed number of **instruction** bytes and representing a length of said potential instruction, wherein each of said position length...

...d'octets de prefixe possibles;un circuit accumulateur de prefixes (310) couple audit circuit de **decodage** et audit **circuit** de recherche de prefixe et configure pour produire une pluralite de vecteurs de longueur de
...a particular instruction byte and represents a length of a potential instruction assuming that the **potential** **instruction** starts at **the particular** **instruction** byte;a **prefix** find circuit configured to receive said fixed number of instruction bytes and to identify which...

...in the set of possible prefix byte values;a prefix accumulator

circuit
coupled to said **decode** circuit and **said** **prefix** find circuit and configured to output a plurality of position length vectors which identify
an...

...instruction length vectors and are adjusted by said identified prefixes;
anda tree circuit coupled **to** said **prefix** accumulation **circuit** and configured to generate and output a plurality of start bits based on the
position...

14/69,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009807242 - Drawing available
WPI ACC NO: 2000-096950/200008
Related WPI Acc No: 2000-062777
XRPX Acc No: N2000-074911
MPEG based variable length decoder for digital versatile disk and digital
video broadcasting set-top-box applications
Patent Assignee: BOSE S (BOSE-I); BUBLIL M (BUBL-I); GADRE S C (GADR-I);
HONG J (HONG-I); OZCELIK T (OZCE-I); SONY CORP (SONY); SONY ELECTRONICS INC (SONY)
Inventor: BOSE S; BUBLIL M; GADRE S C; HONG J; OZCELIK T; GADERE S C
Patent Family (13 patents, 85 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1999060521	A2	19991125	WO 1999US10659	A	19990514	200008	B
AU 199939908	A	19991206	AU 199939908	A	19990514	200019	E
EP 1078533	A2	20010228	EP 1999923050	A	19990514	200113	E
			WO 1999US10659	A	19990514		
CN 1302512	A	20010704	CN 1999806441	A	19990514	200158	E
KR 2001043480	A	20010525	KR 2000712555	A	20001109	200168	E
JP 2002516501	W	20020604	WO 1999US10659	A	19990514	200239	E
			JP 2000550062	A	19990514		
EP 1078533	B1	20030226	EP 1999923050	A	19990514	200316	E
			WO 1999US10659	A	19990514		
US 20030043917	A1	20030306	US 199885797	P	19980518	200320	E
			US 1999280437	A	19990329		
DE 69905565	E	20030403	DE 69905565	A	19990514	200330	E
			EP 1999923050	A	19990514		
			WO 1999US10659	A	19990514		
US 6704361	B2	20040309	US 199885797	P	19980518	200418	E
			US 1999280437	A	19990329		
US 6934338	B1	20050823	US 199885797	P	19980518	200556	E
			US 1999280437	A	19990329		
			US 2003419507	A	20030421		
			US 2003662645	A	20030915		
IN 200000417	P3	20050715	WO 1999US10659	A	19990514	200574	E
			IN 2000MN417	A	20000920		
CN 1199472	C	20050427	CN 1999806441	A	19990514	200641	E

Priority Applications (no., kind, date): US 2003662645 A 20030915; US 2003419507 A 20030421; US 199885797 P 19980518; US 1999280437 A 19990329

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1999060521	A2	EN	58	6	

National Designated States,Original: AE AL AM AT AU AZ BA BB BG BR BY CA
CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG

SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH
GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 199939908	A	EN		Based on OPI patent WO 1999060521
EP 1078533	A2	EN		PCT Application WO 1999US10659 Based on OPI patent WO 1999060521

Regional Designated States,Original: AT BE CH CY DE DK ES FI FR GB GR IE
IT LI LU MC NL PT SE

JP 2002516501	W	JA	90	PCT Application WO 1999US10659 Based on OPI patent WO 1999060521
EP 1078533	B1	EN		PCT Application WO 1999US10659 Based on OPI patent WO 1999060521

Regional Designated States,Original: DE FR GB NL

US 20030043917	A1	EN		Related to Provisional US 199885797
DE 69905565	E	DE		Application EP 1999923050 PCT Application WO 1999US10659 Based on OPI patent EP 1078533 Based on OPI patent WO 1999060521
US 6704361	B2	EN		Related to Provisional US 199885797
US 6934338	B1	EN		Related to Provisional US 199885797 Division of application US 1999280437 Continuation of application US 2003419507
IN 200000417	P3	EN		Division of patent US 6704361 PCT Application WO 1999US10659

Alerting Abstract WO A2

NOVELTY - A command decode and execution circuit (136) coupled to memory (114), receives selected variable length encoded data stored in memory. A sequence (134) provides commands to a circuit to convert the encoded data into corresponding decoded values. A master controller provides commands to the circuit independently to the sequences to control decoding operation of the circuit.

DESCRIPTION - The sequencer includes a memory (140) for storing instructions and an instruction decode and control circuit coupled to the memory for decoding instructions from the memory and then provides commands to the command decode and execution circuit to convert the variable length encoded data into corresponding decoded values.

USE - For decoding digitally encoded video signal transmitted and received in digital audio/video reception in digital versatile disk (DVD) and digital video broadcasting (DVB) set-top-box (STB) applications.

ADVANTAGE - Minimizes amount of memory required to decode the various MPEG variable length codes.

DESCRIPTION OF DRAWINGS - The figure shows block diagram of video decoder.

114,140 Memories
134 Sequence
136 Circuit
142 Control circuit

Technology Focus

INDUSTRIAL STANDARDS - Variable length video decoder is scuted for decoding MPEG-1 and 2 syntax compliant video bit streams.

Title Terms/Index Terms/Additional Words: BASED; VARIABLE; LENGTH; DECODE;
DIGITAL; VERSATILE; DISC; VIDEO; BROADCAST; SET; TOP; BOX; APPLY

Class Codes

International Classification (Main): H04N-007/12, H04N-007/30, H04N-007/50
(Additional/Secondary): H03M-007/42
International Classification (+ Attributes)

IPC + Level Value	Position	Status	Version
G06T-0009/00 A	I	R	20060101
H04N-0007/26 A	I	R	20060101
H04N-0007/30 A	I	R	20060101
H04N-0007/50 A	I	R	20060101
G06T-0009/00 C	I	R	20060101
H04N-0007/26 C	I	R	20060101
H04N-0007/30 C	I	R	20060101
H04N-0007/50 C	I	R	20060101

US Classification, Issued: 382233000, 375240250, 375240230, 375240230

File Segment: EPI;
DWPI Class: S03; T01; W03; W04
Manual Codes (EPI/S-X): T01-D02; T01-H07C3B; T01-J10D; W03-A16C3; W04-C10A3
; W04-F01F1; W04-P01A4

Original Publication Data by Authority

Original Abstracts:

...for decoding the video data and a set of flow control instructions. A
rotator/barrel **shifter** (158) is provided for making a predetermined number of encoded bits from the video bit...

...length decoding using the MPEG standard variable length code (VLC) tables. The variable length table **decoder** (186) shares a **prefix** pattern
matching scheme **across** all of the VLC tables and organizes the variable
length codes into a series of subtables.Each subtable corresponds to one of
the unique prefix patterns. Variable length **codes** are **decoded** by

identifying a leading pattern in the video data bit stream and, in parallel, accessing...

...length decoding using the MPEG standard variable length code (VLC) tables. The variable length table **decoder** shares a **prefix** pattern matching scheme across all **of** the VLC **tables** and organizes the variable
length codes into a series of subtables. Each subtable corresponds to one
of the unique prefix patterns. Variable length codes are **decoded** by identifying **a** leading pattern in the video data bit stream and, in parallel, accessing the subtable corresponding...

...length decoding using the MPEG standard variable length code (VLC) tables. The variable length table **decoder** shares a **prefix** pattern matching scheme across all of the VLC tables and **organizes** the variable
length codes into a series of subtables. Each subtable corresponds to one
of the unique prefix...

...length decoding using the MPEG standard variable length code (VLC) tables. The variable length table **decoder** **shares** a **prefix** pattern **matching** scheme across all of the VLC tables and organizes the variable
length codes **into** a series **of** subtables. Each subtable corresponds to
one of the unique prefix patterns. Variable length codes are ...for decoding the video data and a set of flow control instructions. A rotator/barrel **shifter** (158) is provided for making a predetermined number of encoded bits from the video bit...

...length decoding using the MPEG standard variable length code (VLC) tables. The variable length table **decoder** (186) shares a **prefix** **pattern** matching scheme across all of the VLC tables and organizes the variable length codes into a series of **subtables** .Each subtable corresponds **to** one of the unique prefix patterns. Variable length codes
are decoded by identifying a leading pattern in the video data ...
Claims:
...variable length code table data comprises a plurality of subtable data
circuits each associated with **a** unique **prefix** pattern in the variable
length codes and independent of the prefix pattern length;a datapath...

...to each of the subtable data circuits; andcontrol circuitry responsive
to the pattern match **circuit** for obtaining a **decoded** value from the subtable data circuit associated with the unique prefix pattern in the variable length codes that matches the identified **prefix** pattern in the
variable length encoded data, and additional data in the variable length
codes...

14/69,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008443213 - Drawing available
WPI ACC NO: 1997-052545/199705
Microprocessor with expanded functionality within existing architecture -
has control unit detecting presence of segment override prefixes in instruction code sequences executed in flat memory mode and using prefix
value to control in- and or external functions
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI); ADVANCED MICRO DEVICES
LTD (ADMI)
Inventor: CHRISTIE D S; DUTTON D J
Patent Family (13 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1996041257	A1	19961219	WO 1996US9986	A	19960607	199705	B
US 5680578	A	19971021	US 1995479782	A	19950607	199748	E
EP 834118	A1	19980408	EP 1996923277	A	19960607	199818	E
			WO 1996US9986	A	19960607		
US 5768574	A	19980616	US 1995481704	A	19950607	199831	E
			US 1997914698	A	19970819		
US 5822778	A	19981013	US 1995474400	A	19950607	199848	E
			US 1997886421	A	19970701		
EP 834118	B1	19990331	EP 1996923277	A	19960607	199917	E
			WO 1996US9986	A	19960607		
DE 69601939	E	19990506	DE 69601939	A	19960607	199924	E
			EP 1996923277	A	19960607		
			WO 1996US9986	A	19960607		
ES 2129271	T3	19990601	EP 1996923277	A	19960607	199928	E
JP 11507453	W	19990629	WO 1996US9986	A	19960607	199936	E
			JP 1997502131	A	19960607		
KR 1999022430	A	19990325	WO 1996US9986	A	19960607	200023	E
			KR 1997708910	A	19971205		
CN 1187255	A	19980708	CN 1996194492	A	19960607	200336	E
			WO 1996US9986	A	19960607		
KR 448675	B	20041213	WO 1996US9986	A	19960607	200525	E
			KR 1997708910	A	19971205		
JP 3698441	B2	20050921	WO 1996US9986	A	19960607	200562	E
			JP 1997502131	A	19960607		

Priority Applications (no., kind, date): US 1997914698 A 19970819; US 1997886421 A 19970701; US 1995481704 A 19950607; US 1995479782 A 19950607; US 1995474400 A 19950607

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1996041257	A1	EN	28	6	

National Designated States,Original: CN JP KR
Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT
LU MC NL PT SE

US 5680578	A	EN	13	6	
EP 834118	A1	EN		0	PCT Application WO 1996US9986

				Based on OPI patent WO 1996041257
Regional Designated States,Original: DE ES FR GB				
US 5768574	A	EN		Continuation of application US 1995481704
US 5822778	A	EN		Continuation of application US 1995474400
EP 834118	B1	EN		PCT Application WO 1996US9986
				Based on OPI patent WO 1996041257
Regional Designated States,Original: DE ES FR GB				
DE 69601939	E	DE		Application EP 1996923277
				PCT Application WO 1996US9986
				Based on OPI patent EP 834118
				Based on OPI patent WO 1996041257
ES 2129271	T3	ES		Application EP 1996923277
				Based on OPI patent EP 834118
JP 11507453	W	JA	39	PCT Application WO 1996US9986
				Based on OPI patent WO 1996041257
KR 1999022430	A	KO	6	PCT Application WO 1996US9986
				Based on OPI patent WO 1996041257
CN 1187255	A	ZH		PCT Application WO 1996US9986
				Based on OPI patent WO 1996041257
KR 448675	B	KO		PCT Application WO 1996US9986
				Previously issued patent KR 99022430
				Based on OPI patent WO 1996041257
JP 3698441	B2	JA	15	PCT Application WO 1996US9986
				Previously issued patent JP 11507453
				Based on OPI patent WO 1996041257

Alerting Abstract WO A1

The microprocessor includes an address translation unit (ATU) (116) generating a physical address from a logical one and a segment value. Several segment registers are coupled to the ATU, one storing the segment value. A control unit coupled to the ATU detects an instruction field indicative of one of the segment registers, and conveys a signal to the ATU indicative of it.

A confirmation register stores a value indicative of a microprocessor address translation mode. A second control unit coupled to the configuration register and the first control unit performs a function dependent on the stored value in the configuration register and on the signal from the first control unit.

ADVANTAGE - Code may be easily ported to processor implementing new functions, while overall nature of instruction set remains unchanged.

Title Terms/Index Terms/Additional Words: MICROPROCESSOR; EXPAND; FUNCTION;

EXIST; ARCHITECTURE; CONTROL; UNIT; DETECT; PRESENCE; SEGMENT; OVERRIDE;

INSTRUCTION; CODE; SEQUENCE; EXECUTE; FLAT; MEMORY; MODE; PREFIX; VALUE;

EXTERNAL

Class Codes
International Classification (Main): G06F-012/00, G06F-012/02, G06F-009/318
, G06F-009/32
US Classification, Issued: 395481000, 395479000, 395567000, 711206000, 711209000, 711208000, 395567000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03C
Original Publication Data by Authority

Original Abstracts:
...to use the prefix value or the value stored in the associated segment
register to **selectively** enable **condition** flag modification for instructions. An instruction which modifies the condition flags and a branch instruction...

...be separated by numerous instructions which do not modify the condition
flags. When the branch **instruction** is **decoded** , **the** condition flags it
depends on may already be available. In another embodiment of the present
...

14/69,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008235479 - Drawing available
WPI ACC NO: 1997-341865/199731
XRPX Acc No: N1997-283572
Microcontroller with code and instruction decoding extensions - in which unused opcode in each of two instruction sets is used as prefix to predetermined instructions in respective instruction set when decoder is operating in one of two predetermined modes
Patent Assignee: INTEL CORP (ITLC)
Inventor: PADWEKAR K A
Patent Family (4 patents, 73 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 1997022922	A1	19970626	WO 1996US18838	A	19961206	199731 B
AU 199714069	A	19970714	AU 199714069	A	19961206	199744 E
TW 434472	A	20010516	TW 1997104325	A	19970403	200170 E
US 6317822	B1	20011113	US 1995573305	A	19951215	200173 E
			US 1997943554	A	19971003	

Priority Applications (no., kind, date): US 1997943554 A 19971003; US 1995573305 A 19951215
Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1997022922	A1	EN	22	5	

National Designated States,Original: AL AM AT AU AZ BA BB BG BR BY CA CH
CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA
UG US UZ VN
Regional Designated States,Original: AT BE CH DE DK EA ES FI FR GB GR IE
IT KE LS LU MC MW NL OA PT SD SE SZ UG

AU 199714069	A	EN	Based on OPI patent	WO 1997022922
TW 434472	A	ZH		
US 6317822	B1	EN	Continuation of application	US 1995573305

Alerting Abstract WO A1
The microcontroller includes an extension to provide additional instructions while maintaining backwards compatibility such that instructions for prior processors retain their functionality using one unused opcode in the opcode map. Binary and source modes are provided for this operation. The instruction set is available in both modes, but decoding is different. In binary mode all instructions for the previous processor keep their encoding.

The additional instructions have an A5H prefix which indicates a single unused opcode. In source mode, some of the instructions from the prior processor known as register instructions have the A5 prefix, which

enable
160 opcodes for other functions. Since the register based instructions of
the processor improve the performance of the instructions they replace, there is no need to use the old register based instructions. Therefore, adding a byte and a state to old register instructions results in negligible penalty. In source mode, the instructions for the new processor
do not require the A5 prefix.

USE/ADVANTAGE - Ensuring compatibility between old and new members of family of microcontroller architectures. Provides address space, code and
instruction encoding extensions to microcontroller architecture which provide backward compatibility with existing microcontroller while allowing
significant performance enhancements.

Title Terms/Index Terms/Additional Words: CODE; INSTRUCTION; DECODE; EXTEND
; TWO; SET; PREFIX; PREDETERMINED; RESPECTIVE; OPERATE; ONE; MODE

Class Codes
International Classification (Main): G06F-009/30
US Classification, Issued: 712209000, 712210000, 712229000
File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03; T01-F03C

...**opcode in each of two instruction sets is used as prefix to predetermined instructions in** respective instruction **set when** decoder
is operating in one of two predetermined modes

Original Publication Data by Authority

Claims:
...of opcodes;wherein when said instruction decoder operates in said first
mode, said unused opcode **is used** as a **prefix** that is affixed **individually** to at least a portion of said second plurality of opcodes that is used in...

14/69,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006920064 - Drawing available
WPI ACC NO: 1994-316487/199439
XRPX Acc No: N1994-248596
Pipelined microprocessor including pre-fetch unit - has decoder having prefix state machine for decoding prefixes and determining their lengths and micro-controller for sequencing microcode vectors
Patent Assignee: INTEL CORP (ITLC)
Inventor: ZAIDI S A A
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5353420	A	19941004	US 1992927707	A	19920810	199439 B

Priority Applications (no., kind, date): US 1992927707 A 19920810

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5353420	A	EN	12	4	

Alerting Abstract US A
The pipelined microprocessor includes a prefetch unit for obtaining a plurality of instructions to be processed. A **decode** unit has a **prefix** state machine for **decoding** **prefixes** and determining their lengths. A decode circuit decodes instructions and generates microcode vectors to be executed. An apparatus counts the length of an instruction and a microcontroller sequences microcode vectors. An apparatus for detecting the appearance of a particular prefixed instruction.
An apparatus responsive to the detection of the particular prefixed instruction disables the prefix state machine. An apparatus in the decode circuit **decodes** the particular **prefixed** instruction and causes the decode circuit to generate microcode vectors for the instruction. A request is generated to the microcontroller to handle microcode vectors generated.
USE/ADVANTAGE - For microprocessor running Intel instruction set. Operation of microprocessor is accelerated. Delay due to prefixed jump instructions eliminated.

Title Terms/Index Terms/Additional Words: PIPE; MICROPROCESSOR; PRE; FETCH; UNIT; DECODE; PREFIX; STATE; MACHINE; DETERMINE; LENGTH; MICRO; CONTROL; SEQUENCE; VECTOR

Class Codes
International Classification (Main): G06F-009/38
US Classification, Issued: 395375000, 364231800, 364948340

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B; T01-M02C2

...**has** decoder **having** prefix **state machine for** decoding prefixes **and determining their lengths and micro-controller for sequencing microcode vectors**

Alerting Abstract ...microprocessor includes a prefetch unit for obtaining a plurality of instructions to be processed. A **decode** unit has a **prefix** state machine for **decoding** **prefixes** and determining their lengths. A decode circuit decodes instructions and generates microcode vectors to be...

...the particular prefixed instruction disables the prefix state machine. An apparatus in the decode circuit **decodes** the particular **prefixed** instruction and causes the decode circuit to generate microcode vectors for the instruction. A request...

Original Publication Data by Authority

Original Abstracts:
...which includes a prefetch unit for obtaining a plurality of instructions to be processed; a **decode** unit having a **prefix** state machine for **decoding** **prefixes** and determining **their** **lengths** , a **decode** circuit for decoding instructions and generating microcode vectors to be executed, and apparatus for counting...

...to the detection of the particular prefixed instruction for disabling the prefix state machine, apparatus **in** the **decode** circuit for **decoding** **the** **particular** prefixed **instruction** and **causing** **the** **decode** circuit to generate microcode vectors for the instruction, and apparatus for generating a request to...

Claims:
...which includes a prefetch unit for obtaining a plurality of instructions to be processed; a **decode** unit **having** a **prefix** state **machine** for **decoding** **prefixes** **to** **instructions** and determining their lengths, a decode circuit for decoding instructions and generating microcode vectors to...

...means responsive to the detection of the particular prefixed instruction
for disabling the prefix state **machine** , means in the **decode** circuit **for** decoding the **particular prefixed instruction and causing** the
decode circuit to generate microcode vectors for the instruction, and means for generating a request to...

23/69,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010699503 - Drawing available
WPI ACC NO: 2001-309751/200133
Related WPI Acc No: 2001-309752; 2002-646766
XRPX Acc No: N2001-221751
Processor with reduced latencies associated with branch instructions includes address registers, instruction decoder and execution unit
Patent Assignee: HITACHI LTD (HITA); KRISHNAN S (KRIS-I); ZLESLER S H (ZLES-I)
Inventor: IRIE N; IRLE N; KRISHNAN S; WERNER T L; ZIESLER S H; ZLESLER S H
Patent Family (13 patents, 29 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 1089169	A2	20010404	EP 2000308561	A	20000929	200133	B
JP 2001142705	A	20010525	JP 2000278486	A	20000913	200136	E
KR 2001050791	A	20010625	KR 200057683	A	20000930	200172	E
US 6324643	B1	20011127	US 1999410507	A	19991001	200175	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000679471	A	20001004		
US 6356997	B1	20020312	US 1999410507	A	19991001	200221	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000679131	A	20001004		
US 6374348	B1	20020416	US 1999410507	A	19991001	200232	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000690340	A	20001017		
US 6389531	B1	20020514	US 1999410507	A	19991001	200239	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000690500	A	20001017		
US 6446197	B1	20020903	US 1999410507	A	19991001	200260	E
US 6477639	B1	20021105	US 1999410507	A	19991001	200276	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000679593	A	20001004		
US 20030070062	A1	20030410	US 1999410507	A	19991001	200327	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000679593	A	20001004		
			US 2002288343	A	20021104		
TW 502212	A	20020911	TW 2000120408	A	20000930	200336	E
US 6772323	B2	20040803	US 1999410507	A	19991001	200451	E
			US 1999410682	A	19991001		
			US 1999411340	A	19991001		
			US 2000679593	A	20001004		
			US 2002288343	A	20021104		
KR 2005107318	A	20051111	KR 200591882	A	20050930	200652	E

Priority Applications (no., kind, date): US 2002288343 A 20021104; US 2000690500 A 20001017; US 2000690340 A 20001017; US 2000679593 A 20001004; US 2000679471 A 20001004; US 2000679131 A 20001004; US

1999411340 A 19991001; US 1999410682 A 19991001; US 1999410507 A 19991001

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 1089169	A2	EN	44	4	
Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001142705	A	JA	41		
US 6324643	B1	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340
US 6356997	B1	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340
US 6374348	B1	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340
US 6389531	B1	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340
US 6477639	B1	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340
US 20030070062	A1	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340
					Continuation of application US 2000679593
					Continuation of patent US 6446197
					Continuation of patent US 6477639
TW 502212	A	ZH			
US 6772323	B2	EN			Continuation of application US 1999410507
					Continuation of application US 1999410682
					Continuation of application US 1999411340

Continuation of application US 2000679593

Continuation of patent US 6446197
Continuation of patent US 6477639

Alerting Abstract EP A2

NOVELTY - The processor includes several address registers and an instruction decoder decoding an instruction supplied to it. The decoder provides control signals according to results of the decoding. An execution unit responsive to the control signal executes the instruction.

DESCRIPTION - The instruction can include a first instruction including an operating code field defining a branch control operation and an address field used for calculating an address for a branch. A first register selection field specifies one of the address registers in which the address is to be stored after it is calculated. A second instruction includes an operation code field defining a branch operation. A second register selection field specifies one of the address registers that stores the address to be used for the branch operation.

INDEPENDENT CLAIMS are included for a machine executable branch control instruction and for a computer program.

USE - For high performance computing systems.

ADVANTAGE - Improves instruction execution. Reduces branch instruction delays in highly pipelined processors. Improved branch operation instruction format that is both powerful and flexibly implemented by pipelined processors.

DESCRIPTION OF DRAWINGS - The figure shows a computing system.

Title Terms/Index Terms/Additional Words: PROCESSOR; REDUCE; ASSOCIATE; BRANCH; INSTRUCTION; ADDRESS; REGISTER; DECODE; EXECUTE; UNIT

Class Codes

International Classification (Main): G06F-009/38
International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
G06F-0009/32	A	I	R	20060101
G06F-0009/38	A	I	R	20060101
G06F-0009/32	C	I	R	20060101
G06F-0009/38	C	I	R	20060101

US Classification, Issued: 712234000, 712238000, 712239000, 712237000, 703026000, 712043000, 712229000, 712237000, 712238000, 712239000, 712237000, 711213000, 712238000, 712239000, 712237000, 712233000, 712238000, 712239000, 712237000, 712233000, 712239000, 712237000, 712208000, 712237000, 712234000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03A; T01-F03B

Original Publication Data by Authority

Original Abstracts:
...optimize instruction execution, based on particular indicators specified
for branch target instructions within a branch **hint buffer** .

...

...an improved instruction buffer, branch target instruction memory, branch
target address memory and instruction decoder **adapted** for handling branch
instructions so as to **reduce latencies** . **A** branch operation uses **both** a program branch control instruction (executed in advance to determine the branch target instruction address...instruction and the program branch control instruction both include separate prediction indicators used by the **instruction decoder** for initiating **a** loading
and speculatively pre-loading of instructions for execution in the processor...
...to register comparisons (including a compare to a zero valued register),
predicate evaluations, etc. A **separate** prediction bit within the branch
instruction **specifies** whether **the** branch is likely to be taken or not
taken to a branch control unit in...
Claims:
...a second instruction including an operation code field defining a branch
operation, and a second **register** selection field for **specifying** one of
the plurality of address registers that stores said address to be used for
the branch operation....constitute a target instruction of a corresponding
program branch, and each have a target address **stored** in **a** target address storage location;(c) an instruction decoder which is configured:[i]for decoding said...

...A processor comprising:a plurality **of dedicated** address **registers**
for storing a plurality of different branch target addresses; andan instruction decoder decoding an...

...a branch, and a first register selection field for specifying one of said plurality of **dedicated** address **registers** in which said branch target address is to be stored after it is calculated; and2) a second instruction including an operation **code** field **defining** a branch operation, a second register selection field for **specifying** one of said
plurality of dedicated address **registers** that stores said branch target address to be used for the branch operation, and a...

...by the processor of said first instruction and said second instruction
is arranged so as **to** reduce **latency** for handling said branch

operation,
and such that resolution of said branch condition is performed during
execution of said second instruction; andfurther wherein the microprocessor
operates with a first mode for executing said first length instruction and
a second mode for executing said second length instruction....

23/69,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009715254
WPI ACC NO: 1999-631855/199954
XRPX Acc No: N1999-466430
Mask and shift instructions **for ATM-type frame - Using logical OR operation on result for destination register**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
RD 422110	A	19990610	RD 1999422110	A	19990520	199954 B

Priority Applications (no., kind, date): RD 1999422110 A 19990520

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
RD 422110	A	EN	2	0	

Alerting Abstract RD A

NOVELTY - Instructions are MASH (mask and shift) and MASHO (mask and shift or). The MASH instruction takes five parameters - source register to get data from, most and least significant number of data to **keep** , shift **direction** and number of bits to shift the selected bit field. The MASHO instruction takes an additional parameter **specifying** the destination **register** . The result of the mask and shift operation is logically or-ed into the destination register, useful when multiple non-contiguous fields need to be concatenated.

USE - Instructions are for ATM or other network frames where the header has to be examined to determine which connection the frame is for.

ADVANTAGE - Instructions simplify the field extraction process.

Title Terms/Index Terms/Additional Words: MASK; SHIFT; INSTRUCTION; ATM; TYPE; FRAME; LOGIC; OPERATE; RESULT; DESTINATION; REGISTER

Class Codes
International Classification (Main): H04L

Mask and shift instructions **for ATM-type frame...**

Alerting Abstract ...parameters - source register to get data from, most and least significant number of data to **keep** , shift **direction** and number of bits to shift the selected bit field. The MASHO instruction takes an additional parameter **specifying** the destination **register** . The result of the mask and shift operation is logically or-ed into the

destination...

23/69,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009611499 - Drawing available
WPI ACC NO: 1999-561202/199947
Related WPI Acc No: 2001-307424
XRPX Acc No: N1999-414657
Instruction decoder in digital data processor system for bit mapped graphics processing
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: GUTTAG K M; READ C J
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5960193	A	19990928	US 1993160112	A	19931130	199947 B
			US 1997922726	A	19970827	

Priority Applications (no., kind, date): US 1993160112 A 19931130; US 1997922726 A 19970827

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5960193	A	EN	130	54	Division of application US 1993160112

Alerting Abstract US A

NOVELTY - A functional signal is output to a functional control input of arithmetic logic unit (230) based on which data at input terminals of ALU are added, when multi-bit digital mask signal from a mask generator (239) is at low level. The data at the terminals are subtracted when the output mask signal is at high level.

DESCRIPTION - When the instruction decoder connected to data registers, arithmetic logic unit (230) and flag register, is responsive to an instruction word, data is output from first and second data register units to first and second data inputs of arithmetic logic unit. A functional signal is output to functional control input of arithmetic logic unit using which data received at the second data input terminal is subtracted from the first. A status decoder (210) of arithmetic logic unit generates status signal indicating whether digital resultant signal obtained as a result of subtraction, is less than zero. When the instruction decoder is responsive to second instruction word, data from third and fourth data register units are supplied to first and second data input terminals of arithmetic logic unit.

USE - For bit mapped graphics processing used in video conference multimedia application, high definition television, color facsimile and digital photography.

ADVANTAGE - Three input arithmetic logic units are provided in one digital graphic processor as a part of microprocessor is formed in single integrated circuit used in image processor.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of digital data processing system.

210 Status decoder
230 Arithmetic logic unit
239 Mask generator

Title Terms/Index Terms/Additional Words: INSTRUCTION; DECODE; DIGITAL; DATA; PROCESSOR; SYSTEM; BIT; MAP; GRAPHIC; PROCESS

Class Codes
International Classification (Main): G06F-009/00
US Classification, Issued: 395562000, 395565000, 364716070

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F

Original Publication Data by Authority

Original Abstracts:
...independent sections (301, 302, 303, 304). A multiple flags register (211) stores status bits of **corresponding** sections controlling the **conditional** addition to or subtraction from a like plurality of running sums. After finishing the subtractions...

Claims:
...of instruction words, said plurality of data registers, said arithmetic logic unit and flags register, **said instruction decoder** receiving **individual instruction words** of said stream of instruction words and responsive **to a first instruction word** to supply data from a first data register of said plurality of data registers to...

23/69,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009003831 - Drawing available
WPI ACC NO: 1998-559651/199848
Related WPI Acc No: 1998-559652; 1998-559653; 1998-559656; 2005-513801
XRPX Acc No: N1998-436424
Graphics processor e.g. for creation of graphical images to be printed or displayed - executes computer instruction set in form of opcode with operand which is, or indicates location data to be processed with data to be processed consist of variable length stream of data
Patent Assignee: AMIES C (AMIE-I); CANON INFORMATION SYSTEMS RES AUSTRALIA (CANO); CANON KK (CANO); GIBSON I (GIBS-I); LONG T M (LONG-I)
Inventor: AMIES C; CHUNG W Y; ELBOURNE T R; GIBSON I; GIBSON I R; GRAHAM S; HIGGINBOTTOM R P; KEVIN C H W; LONG T M; MICHAEL J W; PAUL R H; PROKOP T T; PULVER M; STONEY G; TIMOTHY M L; WEBB M J; WIN Y C; WONG K C; YIP D
Patent Family (40 patents, 28 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 875853	A2	19981104	EP 1998303352	A	19980429	199848	B
AU 199863697	A	19981112	AU 199863697	A	19980429	199906	E
AU 199863698	A	19981112	AU 199863698	A	19980429	199906	E
AU 199863695	A	19981119	AU 199863695	A	19980429	199907	E
AU 199863696	A	19981119	AU 199863696	A	19980429	199907	E
JP 11085963	A	19990330	JP 1998169415	A	19980430	199923	E
JP 11085969	A	19990330	JP 1998169416	A	19980430	199923	E
JP 11122116	A	19990430	JP 1998169417	A	19980430	199928	E
JP 11167627	A	19990622	JP 1998169414	A	19980430	199935	E
AU 717168	B	20000316	AU 199863695	A	19980429	200024	E
AU 717336	B	20000323	AU 199863697	A	19980429	200025	E
AU 200014980	A	20000413	AU 199863697	A	19980429	200028	
NCE							
			AU 200014980	A	20000209		
US 6061749	A	20000509	US 199825744	A	19980218	200030	E
AU 200016349	A	20000511	AU 199863695	A	19980429	200031	
NCE							
			AU 200016349	A	20000211		
US 6118724	A	20000912	US 199825726	A	19980218	200046	E
AU 727990	B	20010104	AU 199863698	A	19980429	200107	E
AU 728882	B	20010118	AU 199863696	A	19980429	200109	E
US 6195674	B1	20010227	US 199825506	A	19980218	200114	E
US 6237079	B1	20010522	US 199825758	A	19980218	200130	E
US 6246396	B1	20010612	US 199825771	A	19980218	200135	E
US 6259456	B1	20010710	US 199825614	A	19980218	200141	E
AU 200133402	A	20010621	AU 199863698	A	19980429	200147	
NCE							
			AU 200133402	A	20010402		
US 6272257	B1	20010807	US 199825613	A	19980218	200147	E
US 6289138	B1	20010911	US 199825725	A	19980218	200154	E
US 20010021971	A1	20010913	US 199825194	A	19980218	200155	E

US 6311258	B1	20011030	US 199825843	A	19980218	200172	E
AU 739533	B	20011018	AU 199863697	A	19980429	200174	
NCE							
			AU 200014980	A	20000209		
US 6336180	B1	20020101	US 199825755	A	19980218	200207	E
AU 200197494	A	20020221	AU 200016349	A	20000211	200221	
NCE							
			AU 200197494	A	20011228		
US 6349379	B2	20020219	US 199825194	A	19980218	200221	E
AU 744329	B	20020221	AU 199863695	A	19980429	200223	
NCE							
			AU 200016349	A	20000211		
US 20020057446	A1	20020516	US 199825768	A	19980218	200237	E
US 6393545	B1	20020521	US 199825755	A	19980218	200241	E
			US 2001873429	A	20010605		
US 6414687	B1	20020702	US 199825507	A	19980218	200248	E
US 6507898	B1	20030114	US 199825770	A	19980218	200313	E
AU 760297	B	20030508	AU 200016349	A	20000211	200337	
NCE							
			AU 200197494	A	20011228		
US 6674536	B2	20040106	US 199825768	A	19980218	200411	E
US 6707463	B1	20040316	US 199825614	A	19980218	200420	E
			US 2000611978	A	20000706		
JP 2005348410	A	20051215	JP 1998169417	A	19980430	200582	E
			JP 2005161916	A	20050427		
EP 875855	B1	20060802	EP 1998303363	A	19980429	200651	E

Priority Applications (no., kind, date): AU 200197494 A 20011228; AU 200133402 A 20010402; AU 200016349 A 20000211; AU 200014980 A 20000209; AU 19976492 A 19970430; AU 19976491 A 19970430; AU 19976490 A 19970430; AU 19976489 A 19970430; AU 19976488 A 19970430; AU 19976487 A 19970430; AU 19976486 A 19970430; AU 19976485 A 19970430 ; AU 19976484 A 19970430; AU 19976483 A 19970430; AU 19976482 A 19970430; AU 19976481 A 19970430; AU 19976480 A 19970430; AU 19976479 A 19970430

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 875853	A2	EN	333	158	

Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

JP 11085963	A	JA	684		
JP 11085969	A	JA	719		
JP 11122116	A	JA	748		
JP 11167627	A	JA	821		
AU 717168	B	EN		Previously issued patent	AU 9863695
AU 717336	B	EN		Previously issued patent	AU 9863697
AU 200014980	A	EN		Division of application	AU 199863697

				Division of patent AU 717336
AU 200016349 199863695	A	EN		Division of application AU
				Division of patent AU 717168
AU 727990 9863698	B	EN		Previously issued patent AU
AU 728882 9863696	B	EN		Previously issued patent AU
AU 200133402 199863698	A	EN		Division of application AU
				Division of patent AU 727990
AU 739533 199863697	B	EN		Division of application AU
				Previously issued patent AU
200014980				
				Division of patent AU 717336
AU 200197494 200016349	A	EN		Division of application AU
				Division of patent AU 744329
AU 744329 199863695	B	EN		Division of application AU
				Previously issued patent AU
200016349				
				Division of patent AU 717168
US 6393545 199825755	B1	EN		Continuation of application US
				Continuation of patent US 6336180
AU 760297 200016349	B	EN		Division of application AU
				Previously issued patent AU
200197494				
				Division of patent AU 744329
US 6707463 199825614	B1	EN		Division of application US
JP 2005348410 1998169417	A	JA	328	Division of application JP
EP 875855	B1	EN		

Regional Designated States,Original: DE FR GB

Alerting Abstract EP A2

The processor comprises several interrelated functional modules. A register is associated with each of the functional modules. Each register is configured to control the function of its associated functional module.

An instruction controller decodes instructions for use with the graphics
processor, the instruction controller includes a register setting device to
set the registers in accordance with a decoded instruction, to configure
the function of each of the functional modules in response to each instruction.

The registers include a semaphore access mechanism accessible by external
modules,including the functional modules. Some of the functional registers
include a status register, the contents of each of which is updateable by
its associated register during or following execution of an instruction.

ADVANTAGE - Facilitates processing of variable length streams of data.

Title Terms/Index Terms/Additional Words: GRAPHIC; PROCESSOR; CREATION; GRAPHICAL; IMAGE; PRINT; DISPLAY; EXECUTE; COMPUTER; INSTRUCTION; SET; FORM; OPERAND; INDICATE; LOCATE; DATA; PROCESS; CONSIST; VARIABLE; LENGTH ; STREAM

Class Codes

International Classification (Main): G06T-001/00, G06T-001/20, G06T-009/00, H03M-007/40

(Additional/Secondary): G06F-012/08, G06T-011/80, H04N-001/387, H04N-001/41, H04N-001/46, H04N-001/60, H04N-007/24, H04N-007/30, H04N-007/50, G06F-015/16, G06F-017/14, H03M-007/30

International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
G06F-0012/00	A	I	R	20060101
G06F-0015/167	A	I	R	20060101
G06F-0009/28	A	I	R	20060101
G06F-0009/30	A	I	R	20060101
G06F-0009/38	A	I	R	20060101
G06F-0009/38	A	I L	B	20060101
G06T-0001/20	A	I F	B	20060101
G06T-0001/20	A	I	R	20060101
G06T-0001/60	A	I	R	20060101
G06T-0011/00	A	I	R	20060101
G06T-0015/00	A	I	R	20060101
G06T-0007/00	A	I	R	20060101
G06T-0009/00	A	I	R	20060101
G11C-0008/00	A	I	R	20060101
H03M-0007/30	A	I	R	20060101
H03M-0007/40	A	I	R	20060101
H04N-0007/50	A	I	R	20060101
G06F-0012/00	C	I	R	20060101
G06F-0015/16	C	I	R	20060101
G06F-0009/28	C	I	R	20060101
G06F-0009/30	C	I	R	20060101
G06F-0009/38	C	I	R	20060101

G06T-0001/20 C I R 20060101
G06T-0001/60 C I R 20060101
G06T-0011/00 C I R 20060101
G06T-0015/00 C I R 20060101
G06T-0007/00 C I R 20060101
G06T-0009/00 C I R 20060101
G11C-0008/00 C I R 20060101
H03M-0007/30 C I R 20060101
H03M-0007/40 C I R 20060101
H04N-0007/50 C I R 20060101

US Classification, Issued: 712215000, 358001150, 358001160, 382307000, 358001130, 708204000, 708205000, 345154000, 710065000, 365189020, 365221000, 365230020, 365230050, 708401000, 708402000, 711153000, 712034000, 345153000, 345154000, 345513000, 358523000, 358524000, 358525000, 345186000, 345501000, 345433000, 382246000, 382308000, 382307000, 711210000, 711211000, 711212000, 711214000, 711215000, 711200000, 711206000, 711207000, 711209000, 712034000, 712225000, 712210000, 712035000, 711148000, 711153000, 711163000, 712034000, 345520000, 345559000, 712032000, 712033000, 712229000, 345503000, 711118000, 711168000, 358001900, 358001150, 345501000, 345619000

File Segment: EngPI; EPI;
DWPI Class: T01; P85
Manual Codes (EPI/S-X): T01-F03C; T01-J10B; T01-M02

Original Publication Data by Authority

Original Abstracts:

...co-processor instructions to be executed, and those which have been executed are allocated to **respective queues** (1040, 1041). From
time to time the latter queue (1041) is cleaned up under control...

...the co-processor by the CPU. This dynamic memory management arrangement
preferably includes an instruction **generator** (**1030**), a memory
manager (1031) and a queue manager (1032...variable length
stream of data and each instruction includes a length field (297)
containing data **specifying the** number of items of data to be processed
or, if that number exceeds the size...

...for use with the graphics processor. The control bus and the data pipeline are physically **separate** , and the **instruction** controller includes a register setting unit adapted to set the registers via the control bus ...

Claims:

...memory array; anda plurality of first-in-first-out (FIFO) output buffers
coupled to **respective** ones of **said** plurality of read ports, wherein said FIFO output buffers are disposed between said memory array...

...from said memory array, and each of said read ports is de-coupled by

its
respective FIFO output **buffer** from said memory array and/or a plurality
of first-in-first-out (FIFO) input...

...to said memory array, and each of said write ports is de-coupled by its
respective FIFO input **buffer** from said memory array...

...including a combinatorial circuit for calculating a DCT without a clocked storage unit.

...

...of controlling the interaction between a host CPU and at least one co-processor in **a** computer system **to** permit substantially simultaneous
decoupled execution of CPU instructions and co-processor instructions, and
dynamic allocation ...enabling or disabling a plurality of options in said
image processing operation;a configuration register **for** storing said image processing operation **and** options;a register file **for** storing information necessary for performing said image processing
operation;decoding means connected to said configuration r... A data store **apparatus** adapted to **store** first data objects comprised of **a** plurality of first data items and to store second data objects comprised of
one or...

...the calculation represents processed image data, and each instruction
includes a length field that includes **data** specifying a **number** of items
of data to be processed or, if the number exceeds a size of...of the registers for conveying instructions, wherein said control bus and the data
pipeline are **physically** separate; and **an** instruction controller **for decoding** instructions for use with the graphics processor, the instruction
controller including a register setting unit...

23/69,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008745016 - Drawing available
WPI ACC NO: 1998-287185/199825
XRPX Acc No: N1998-225670
Eight-bit microcontroller with RISC architecture - has direct-address bus couples program execution unit to directly access data store and register file during program execution, indirect-address bus provides register file with indirect data access to data store during program execution
Patent Assignee: ATMEL CORP (ATME-N)
Inventor: BOGEN A; BRYANT D; BRYANT J D; MYKLEBUST G; WOLLAN V

Patent Family (14 patents, 23 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1998020422	A1	19980514	WO 1997US19626	A	19971030	199825	B
US 5854939	A	19981229	US 1996745098	A	19961107	199908	E
TW 355772	A	19990411	TW 1997116599	A	19971107	199935	E
EP 954791	A1	19991110	EP 1997913860	A	19971030	199952	E
			WO 1997US19626	A	19971030		
CN 1236455	A	19991124	CN 1997199485	A	19971030	200014	E
KR 2000053047	A	20000825	WO 1997US19626	A	19971030	200121	E
			KR 1999703950	A	19990504		
JP 2001504959	W	20010410	WO 1997US19626	A	19971030	200128	E
			JP 1998521534	A	19971030		
EP 954791	B1	20050316	EP 1997913860	A	19971030	200522	E
			WO 1997US19626	A	19971030		
			EP 200429045	A	19971030		
DE 69732793	E	20050421	DE 69732793	A	19971030	200528	E
			EP 1997913860	A	19971030		
			WO 1997US19626	A	19971030		
KR 465388	B	20050113	WO 1997US19626	A	19971030	200535	E
			KR 1999703950	A	19990504		
CN 1115631	C	20030723	CN 1997199485	A	19971030	200548	E
JP 3694531	B2	20050914	WO 1997US19626	A	19971030	200560	E
			JP 1998521534	A	19971030		
EP 1596279	A2	20051116	EP 1997913860	A	19980514	200575	E
			EP 200429045	A	19971030		
DE 69732793	T2	20060406	DE 69732793	A	19971030	200625	E
			EP 1997913860	A	19971030		
			WO 1997US19626	A	19971030		

Priority Applications (no., kind, date): US 1996745098 A 19961107

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1998020422	A1	EN	44	6	

National Designated States,Original: CN DE GB JP KR
Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT
LU MC NL PT SE

TW 355772	A	ZH	
EP 954791	A1	EN	PCT Application WO 1997US19626 Based on OPI patent WO 1998020422

Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT
LI LU NL PT SE

KR 2000053047 A KO 10 PCT Application WO 1997US19626
Based on OPI patent WO 1998020422

JP 2001504959 W JA 46 PCT Application WO 1997US19626
Based on OPI patent WO 1998020422

EP 954791 B1 EN PCT Application WO 1997US19626
Related to application EP 200429045
Based on OPI patent WO 1998020422
Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT
LI LU NL PT SE

DE 69732793 E DE Application EP 1997913860
PCT Application WO 1997US19626
Based on OPI patent EP 954791
Based on OPI patent WO 1998020422

KR 465388 B KO PCT Application WO 1997US19626
Previously issued patent KR 2000053047
Based on OPI patent WO 1998020422

JP 3694531 B2 JA 22 PCT Application WO 1997US19626
Previously issued patent JP 2001504959
Based on OPI patent WO 1998020422

EP 1596279 A2 EN Division of application EP 1997913860
Division of patent EP 954791
Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT
LI LU NL PT SE

DE 69732793 T2 DE Application EP 1997913860
PCT Application WO 1997US19626
Based on OPI patent EP 954791
Based on OPI patent WO 1998020422

Alerting Abstract WO A1

The system includes a program store for storing programs and a program execution unit is coupled to the program store via a program bus. A data store separate from the program store is coupled to the eight-bit data bus. A register file is coupled to the eight-bit data bus and has a number of eight-bit registers. The register file combines two of the eight-bit registers to be accessed as a single logical sixteen-bit register. A general purpose ALU is coupled to receive the contents of two of the eight-bit registers, and has an output coupled to the eight-bit data bus. A direct-address bus couples the program execution unit to **directly** access the data **store** and the register file during program execution. An

indirect-address bus provides the register file with indirect data access
to the data store during program execution. A dedicated ALU performs arithmetic functions on a logical sixteen-bit register accessed through the
combining device.
ADVANTAGE - Provides complete and efficient instruction set for application software developer.

Title Terms/Index Terms/Additional Words: EIGHT; BIT; ARCHITECTURE; DIRECT;
ADDRESS; BUS; COUPLE; PROGRAM; EXECUTE; UNIT; ACCESS; DATA; STORAGE; REGISTER; FILE; INDIRECT

Class Codes
International Classification (Main): G06F-013/00, G06F-009/30, G06F-009/32,
G06F-009/34, G06F-009/345
(Additional/Secondary): G06F-009/302, G06F-009/355
International Classification (+ Attributes)
IPC + Level Value Position Status Version
G06F-0013/00 A I F B 20060101
G06F-0009/30 A I L B 20060101
G06F-0009/302 A I L B 20060101
G06F-0009/355 A I L B 20060101
G06F-0009/34 C I L B 20060101
US Classification, Issued: 395800410, 395800010, 395800310, 395800320, 395800330

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-M05

...has direct-address bus couples program execution unit to directly access data store and register file during program execution, indirect-address bus provides register file with indirect data...

Alerting Abstract ...the eight-bit data bus. A direct-address bus couples
the program execution unit to **directly** access the data **store** and the
register file during program execution. An indirect-address bus provides
the register file...

Original Publication Data by Authority

Original Abstracts:
An eight-bit RISC based microcontroller (10) includes an eight-bit register
file having a **dedicated** arithmetic logic unit ALU (ALU-2), in addition to
general purpose eight-bit ALU (ALU...

...within the register file with a single instruction. This avoids having

to perform various loads, **shift** **and** /or masking operations needed by prior art microcontrollers...

...a dedicated arithmetic logic unit (ALU), in addition to a general purpose eight-bit ALU. **The** **register** file further includes means for combining a pair of registers to provide a logical sixteen-bit register for
indirect addressing. The **dedicated** ALU **is** a sixteen-bit ALU which provides certain arithmetic functions for the **register** pair, thus alleviating the computational burdens that would otherwise be imposed on
the general purpose...
Claims:
...einem vom Programmspeicher separaten Datenspeicher (SRAM), der mit dem
Acht-Bit-Datenbus (12) gekoppelt ist; **einer** **Registerdatei** , die mit dem
Acht-Bit-Datenbus (12) gekoppelt **ist** , wobei die **Registerdatei** eine Vielzahl von Acht-Bit-Registern (R0-R30) aufweist, wobei die Registerdatei
ferner ein Mittel...

...bit data bus (12);a direct-address bus (16) coupling said program execution unit to **directly** access said data **store** (SRAM) and said register file during program execution; characterized byan indirect-address bus (14...

...ALU (ALU-2) coupled to said combining means in order to perform arithmetic functions on **a** logical sixteen-bit **register** (R27/R26) accessed through said combining means;said indirect-address bus (14) having
address-receiving...said general purpose ALU having an output coupled to
said eight-bit data bus;a **direct** -address bus **coupling** said program execution unit to **directly** access said data **store** and **said** **register**
file during program execution; andan indirect-address **bus** providing said
register file with indirect data access to said randomly accessible memory
during program execution;said register file further including a **dedicated**
ALU **coupled** to said means for combining in order to perform arithmetic
functions on a logical sixteen

23/69,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008610995 - Drawing available
WPI ACC NO: 1998-147173/199814
XRPX Acc No: N1998-116613
Super-scalar architecture processor - has multiplex-controlled paradigm unit for dynamic re-configuration and programming during execution of program
Patent Assignee: INFINEON TECHNOLOGIES AG (INFN); SIEMENS AG (SIEI)
Inventor: SIEMERS C; SIEMERS C R
Patent Family (8 patents, 26 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 825540	A1	19980225	EP 1997114501	A	19970821	199814	B
DE 19634031	A1	19980226	DE 19634031	A	19960823	199814	E
JP 10105402	A	19980424	JP 1997238917	A	19970820	199827	E
KR 1998018874	A	19980605	KR 199740002	A	19970822	199923	E
US 6061367	A	20000509	US 1997918282	A	19970825	200030	E
KR 316078	B	20020112	KR 199740002	A	19970822	200254	E
EP 825540	B1	20030507	EP 1997114501	A	19970821	200333	E
DE 59710022	G	20030612	DE 59710022	A	19970821	200340	E
			EP 1997114501	A	19970821		

Priority Applications (no., kind, date): EP 1997114501 A 19970821; DE 19634031 A 19960823

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 825540	A1	DE	18	11	

Regional Designated States,Original: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC NL PT RO SE SI

DE 19634031	A1	DE	18		
JP 10105402	A	JA	12		
KR 1998018874	A	KO		12	
KR 316078	B	KO			Previously issued patent KR 98018874
EP 825540	B1	DE			

Regional Designated States,Original: DE FR GB IT

DE 59710022	G	DE	Application EP 1997114501 Based on OPI patent EP 825540

Alerting Abstract EP A1

The processor has a programmable structure buffer (30) acting as a logic unit, an integer/address instruction buffer (32), an integer register file (24) for direct communication with a data storage interface (36) and a functional unit (34) with a programmable structure forming a multiplex-controlled paradigm unit for dynamic re-configuration/programming during execution of the program.

The functional unit uses a number of arithmetic units, a number of compare units, multiplexers, inserted between the arithmetic units, the

compare units and the register file and demultiplexers between the outputs
of the compare units and the arithmetic units.
USE - For superscalar microcomputer.
ADVANTAGE - Programmable structure allows optimum use of resources for
maximum processing rate.

Title Terms/Index Terms/Additional Words: SUPER; SCALE; ARCHITECTURE; PROCESSOR; MULTIPLEX; CONTROL; UNIT; DYNAMIC; CONFIGURATION; PROGRAM; EXECUTE

Class Codes
International Classification (Main): G06F-015/78, G06F-009/28, G06F-009/38,
H04J-003/04
(Additional/Secondary): G01B-011/22, G06F-015/80, G06F-009/302, G06F-009/45
US Classification, Issued: 370535000, 712033000
File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B1; T01-M02C2; T01-S01A

Original Publication Data by Authority

Original Abstracts:
...processor having a pipelining structure, in particular with a superscalar architecture, includes a configurable logic **unit** , an **instruction** memory, a **decoder** unit, an interface device, a programmable
structure buffer, an integer/address instruction buffer and a...
Claims:
...unit (18), an integer/address instruction buffer (32) and an integer register file (24) for **direct** communication with data- **storing** interface
means (36),</br>characterized bya functional unit with a programmable structure (34), havinga...output busses, which are provided
between the arithmetic units (50, 51), the compare units (52) **and** the **register** file (24), as well asa plurality of demultiplexers (46) having
one input bit and a plurality of output bits, for delivery of the results
of the comparisons (CoU) **in** a destination selection to corresponding arithmetic units (50, 51),a multiplex-controlled s-paradigm unit...

23/69,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008356746 - Drawing available
WPI ACC NO: 1997-470414/199743
XRPX Acc No: N1997-392542
Data processor for executing instructions to insert or extract data to or from optional byte position of register - specifies bit area on destination register by decoding instruction contg. operation code, source operand and destination operand, and inserts source data in register or memory into specified area
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)

Inventor: DOI T; IWATA S; MIZUGAKI S; SHIMIZU T
Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 5669012	A	19970916	US 1994245792	A	19940519	199743	B
			US 1996720455	A	19960930		
JP 3203401	B2	20010827	JP 1993120014	A	19930521	200152	E
JP 2001356902	A	20011226	JP 1993120014	A	19930521	200206	E
			JP 2001130294	A	19930521		

Priority Applications (no., kind, date): JP 2001130294 A 19930521; JP 1993120014 A 19930521

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5669012	A	EN	25	18	Continuation of application US 1994245792
JP 3203401	B2	JA	15		Previously issued patent JP 06332695
JP 2001356902	A	JA	14		Division of application JP 1993120014

Alerting Abstract US A

The data processor has a micro-decoder which decodes instruction codes comprising two operation code parts, a source operand specifying part and a destination operand specifying part. An optional bit area of source data - a register of a general register file or a memory - is inserted in an optional bit area, determined by the value of the first operation code part, of a destination register according to the decoding result.

An optional bit area, determined by the value of the second operation code part, of a source register is extracted and **stored** in an **optional** bit area of destination - a register of the general register file or the

memory.
ADVANTAGE - Processes insertion and extraction operations to and from optional byte positions of registers at high speed with short instruction
code size.

Title Terms/Index Terms/Additional Words: DATA; PROCESSOR; EXECUTE; INSTRUCTION; INSERT; EXTRACT; OPTION; BYTE; POSITION; REGISTER; SPECIFIED
; BIT; AREA; DESTINATION; DECODE; CONTAIN; OPERATE; CODE; SOURCE; OPERAND
; MEMORY

Class Codes
International Classification (Main): G06F-009/30, G06F-009/305, G06F-009/35
(Additional/Secondary): G06F-007/00, G06F-009/34
US Classification, Issued: 395800010, 395376000, 395384000, 395390000, 395611000, 395670000, 395898000, 364DIG001

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-E02D; T01-F01C; T01-F03A; T01-H01D; T01-J10B;
T01-S01A

Alerting Abstract ...the value of the second operation code part, of a
source register is extracted and **stored** in an **optional** bit area of destination - a register of the general register file or the memory...

Original Publication Data by Authority

Original Abstracts:
...the value of the second operation code part) of a source register is extracted and **stored** in an **optional** **bit** area of **destination** (a register of the general register file or the memory), thereby making it possible to...
Claims:
...data to or from an optional byte position of a register, the data processor comprising: **instruction** **decoding** means for **decoding** **a** digital **instruction** **code** including a **source** operand **specifying** part, a destination operand specifying part, information specifying a byte
position in the source operand...

...decoding result specifying a source data corresponding to said source
operand specifying part, a memory **or** destination **register** corresponding
to said destination operand specifying part, a position in the source data
corresponding to...

...comprising one or a plurality of bits, corresponding to said operation

specifying part; a memory **and** a **register** file having one or a plurality
of registers, at least one of the memory and the one or a plurality of registers being specified as the destination operand by **said decoding**
result; **instruction** executing means, connected to said instruction decoding means and receiving said **decoding** result, **for** **reading** source
data **specified** by said decoding result and inserting a bit string, the
length of which is specified...

...by said decoding result, and storing the resulting source data in the
memory or register **specified** by said **decoding** result; and **instruction**
executing **controlling** means, connected **to** said **instruction** executing
means, for operating said instruction executing means when said operation
specifying part **decoded** by **said** **instruction** **decoding** means is a
predetermined code.

23/69,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007414513 - Drawing available
WPI ACC NO: 1996-022045/199603
XRPX Acc No: N1996-018299
Superscaler microprocessor with flag operand renaming and forwarding - has unit decoding instructions in stream and translating them into ROPs with reorder buffer storing concatenated integer and flag results to form floating point results
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: CHRISTIE D S; GODDARD M D; WHITE S A
Patent Family (8 patents, 14 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 686913	A2	19951213	EP 1995303667	A	19950530	199603	B
JP 7334364	A	19951222	JP 1995134013	A	19950531	199609	E
EP 686913	A3	19961127	EP 1995303667	A	19950530	199702	E
US 5632023	A	19970520	US 1994252029	A	19940601	199726	E
US 5805853	A	19980908	US 1994252029	A	19940601	199843	E
			US 1997799064	A	19970210		
EP 686913	B1	19990317	EP 1995303667	A	19950530	199915	E
DE 69508303	E	19990422	DE 69508303	A	19950530	199922	E
			EP 1995303667	A	19950530		
JP 3662296	B2	20050622	JP 1995134013	A	19950531	200541	E

Priority Applications (no., kind, date): US 1997799064 A 19970210; US 1994252029 A 19940601

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 686913	A2	EN	43	11	
Regional Designated States,Original: AT BE DE DK ES FR GB GR IE IT LU NL PT SE					
JP 7334364	A	JA	37		
EP 686913	A3	EN			
US 5632023	A	EN	36	11	
US 5805853	A	EN			Continuation of application US 1994252029
					Continuation of patent US 5632023
EP 686913	B1	EN			
Regional Designated States,Original: AT BE DE DK ES FR GB GR IE IT LU NL PT SE					
DE 69508303	E	DE			Application EP 1995303667
					Based on OPI patent EP 686913
JP 3662296	B2	JA	47		Previously issued patent JP 07334364

Alerting Abstract EP A2

The microprocessor has a decoder decoding instructions contained in an

instruction stream and translating them once decoded into RISC-like instructions (ROPs). A reorder buffer (35), coupled to the decoder stores
the speculative state of the processor. A register file (30), coupled to
the reorder buffer, stores the real state of the processor.
The reorder buffer includes an array with several storage locations including integer result portions for storing a speculative integer result
and a flag result portion for storing speculative flag information associated with the integer result. The flag result portion and the integer
result portion are concatenated to form a floating point storage location
which accommodates storage of floating point results wider than the integer
results. A real flags register, coupled to the reorder buffer, stores flag
information retired from the reorder buffer.
ADVANTAGE - Flags are advantageously grouped to lessen number of dependency checkers that are needed,. Microprocessor exhibits enhanced performance w.r.t. execution of instructions. Requires small number of flag
structures.

Title Terms/Index Terms/Additional Words: MICROPROCESSOR; FLAG; OPERAND;
FORWARDING; UNIT; DECODE; INSTRUCTION; STREAM; TRANSLATION; BUFFER; STORAGE; CONCATENATED; INTEGER; RESULT; FORM; FLOAT; POINT

Class Codes
International Classification (Main): G06F-009/30, G06F-009/38
US Classification, Issued: 395394000, 395800000, 395391000, 395394000, 395391000, 395800230

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B

Original Publication Data by Authority

Original Abstracts:
...of the microprocessor. To enhance the performance of the microprocessor
with respect to conditional branching **instructions** , the reorder **buffer**
includes a flag storage area for storing flags that are updated by flag modifying instructions...

...of the microprocessor with respect to conditional branching instructions, the reorder buffer includes a flag **storage** area for **storing** flags that are updated by flag modifying instructions. The flags
are renamed to make possible...

...with respect to conditional branching instructions, the reorder

buffer
includes a flag storage area for **storing** flags **that** are updated by flag
modifying instructions. The flags are renamed to make possible the earlier
...
Claims:
...in an instruction stream or for decoding instructions contained in an
instruction stream and translating **decoded** **instructions** into ROPs **respectively** ;</br> **a** reorder **buffer** , **coupled** to the decoder, for
storing the speculative state of the microprocessor;</br> a register file, coupled...

...instructions contained in an instruction stream and translating decoded
instructions into RISC-like operations ("ROPs") **respectively** ;</br> a
reorder **buffer** (285), coupled to the decoder, for storing the speculative
state of the microprocessor;</br> a register file (255), coupled to the
reorder buffer, for storing the real state of the microprocessor;</br> **the** reorder **buffer** (285), including a reorder buffer array having a plurality of storage locations which include an ...

23/69,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007130871 - Drawing available
WPI ACC NO: 1995-163659/199522
Related WPI Acc No: 1996-020202
XRPX Acc No: N1995-128351
Write buffer for super-pipelined super-scalar microprocessor - directs each write to memory to write buffer rather than memory bus or cache memory and writes contents of write buffer to cache or main memory when memory bus or cache becomes available
Patent Assignee: CYRIX CORP (CYRI-N); NAT SEMICONDUCTOR CORP (NASC); VIA-CYRIX INC (VIAC-N)
Inventor: BLUHM M; GARIBAY R; GARIBAY R A; HERVIN M W; MARC; NITARU P; PATWA N; QUATTROMANI M A
Patent Family (10 patents, 10 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 651331	A1	19950503	EP 1994307580	A	19941017	199522	B
JP 7152566	A	19950616	JP 1994251989	A	19941018	199533	E
US 5584009	A	19961210	US 1993138654	A	19931018	199704	E
US 5615402	A	19970325	US 1993138652	A	19931018	199718	E
			US 1995572584	A	19951214		
US 5740398	A	19980414	US 1993138651	A	19931018	199822	E
US 5907860	A	19990525	US 1993138654	A	19931018	199928	E
			US 1996688900	A	19960731		
US 6219773	B1	20010417	US 1993138790	A	19931018	200123	E
EP 651331	B1	20020109	EP 1994307580	A	19941017	200211	E
DE 69429612	E	20020214	DE 69429612	A	19941017	200220	E
			EP 1994307580	A	19941017		
JP 3678443	B2	20050803	JP 1994251989	A	19941018	200551	E

Priority Applications (no., kind, date): US 1996688900 A 19960731; US 1995572584 A 19951214; EP 1994307580 A 19941017; US 1993138596 A 19931018; US 1993139598 A 19931018; US 1993139596 A 19931018; US 1993138790 A 19931018; US 1993138654 A 19931018; US 1993138652 A 19931018; US 1993138651 A 19931018

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 651331	A1	EN	38		
Regional Designated States,Original: CH DE ES FR GB IE IT LI NL					
JP 7152566	A	JA	36		
US 5584009	A	EN	29	18	
US 5615402	A	EN	29	18	Continuation of application US 1993138652
US 5740398	A	EN	29		
US 5907860	A	EN			Continuation of application US 1993138654
EP 651331	B1	EN			
Regional Designated States,Original: CH DE ES FR GB IE IT LI NL					
DE 69429612	E	DE			Application EP 1994307580 Based on OPI patent EP 651331

JP 3678443 B2 JA 43 Previously issued patent JP 07152566

Alerting Abstract EP A1

The microprocessor includes a write buffer located between the CPU and memory cache which stores the results of write operations to memory until the cache memory becomes available, i.e when no high priority reads are to be performed. The write buffer includes multiple entries that are split into two circular buffer sections for facilitating the interaction with the two core pipelines. Cross-dependency tables are provided for each write buffer entry to ensure that the data is written from the write buffer to memory in program order, while considering any prior data in the opposite section.

Non-cacheable reads from memory are also ordered in program order with the writing of data from the write buffer. Features for performing misaligned writes, handling speculative execution, detecting and handling data dependencies and exceptions, and performing gathered writes are also included within the microprocessor.

USE/ADVANTAGE - Memory access in microprocessor. Enables misaligned writes to be easily handled with minimal loss of performance. Ensures retiring of data from write buffer to cache or main memory in program order.

Title Terms/Index Terms/Additional Words: WRITING; BUFFER; SUPER; PIPE; SCALE; MICROPROCESSOR; DIRECT; MEMORY; BUS; CACHE; CONTENT; MAIN; AVAILABLE

Class Codes

International Classification (Main): G06F-012/04, G06F-012/08, G06F-013/00, G06F-009/38
(Additional/Secondary): G06F-012/00

US Classification, Issued: 395444000, 395445000, 395464000, 395449000, 364DIG001, 364261500, 364261700, 395800000, 395250000, 395410000, 395467000, 364704000, 364736000, 364748000, 395444000, 395250000, 395872000, 395449000, 711117000, 711144000, 711118000, 711169000, 395591000, 395872000, 711201000, 710052000

File Segment: EPI;

DWPI Class: T01

Manual Codes (EPI/S-X): T01-H01A; T01-H03A; T01-H05B1; T01-M02C

Original Publication Data by Authority

Claims:

...instruction is a misaligned write instruction;</br> (f) a shifter coupled to the write buffer to **shift** the **contents** of a first entry

of
the plurality of entries detected as **a** misaligned write **instruction** by
the control logic, prior to presentation of the first entry to the cache
memory...

...bits (XDEP), each cross-dependency bit corresponding to one of the buffer entries in the **respective** **second** and first sections (152x, 152y)
and indicating, when set, that the corresponding buffer entry
was...core
for executing data processing operations according to a series of instructions, said microprocessor including **a** write **buffer** having a plurality of write buffer entries for buffering the results of the instructions executed...
...write buffer means having a plurality of entries, coupled to the core
means and the **misalignment** control means, for temporarily **storing** the
plurality of write operands and responsive to the misalignment control means indicating a misaligned...

23/69,K/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005788180 - Drawing available
WPI ACC NO: 1992-010489/199202
XRPX Acc No: N1992-008049
In-register data manipulation in RISC processor - permitting only simplified memory access data width and addressing modes with set limited to register operations
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: SITES R; SITES R L; WITEK R; WITEK R T
Patent Family (10 patents, 7 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 465322	A	19920108	EP 1991401770	A	19910627	199202	B
CA 2045705	A	19911230				199213	E
EP 465322	A3	19921119	EP 1991401770	A	19910627	199342	E
US 5367705	A	19941122	US 1990547619	A	19900629	199501	E
			US 1993117482	A	19930907		
US 5410682	A	19950425	US 1990547619	A	19900629	199522	E
			US 1993117482	A	19930907		
			US 1994289025	A	19940810		
TW 285729	A	19960911	TW 1991106677	A	19910822	199704	E
EP 465322	B1	19990922	EP 1991401770	A	19910627	199943	E
DE 69131637	E	19991028	DE 69131637	A	19910627	199951	E
			EP 1991401770	A	19910627		
JP 3105960	B2	20001106	JP 1991254082	A	19910628	200059	E
KR 231380	B1	19991115	KR 199110879	A	19910628	200111	E

Priority Applications (no., kind, date): US 1994289025 A 19940810; US 1993117482 A 19930907; US 1990547619 A 19900629

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 465322	A	EN			
Regional Designated States,Original: DE FR GB NL					
CA 2045705	A	EN			
EP 465322	A3	EN			
US 5367705	A	EN	22	11	Continuation of application US 1990547619
US 5410682	A	EN	22	11	Continuation of application US 1990547619
					Continuation of application US 1993117482
					Continuation of patent US 5367705
TW 285729	A	ZH			
EP 465322	B1	EN			
Regional Designated States,Original: DE FR GB NL					
DE 69131637	E	DE			Application EP 1991401770
					Based on OPI patent EP 465322
JP 3105960	B2	JA	32		Previously issued patent JP 06119166

Alerting Abstract EP A

The method of byte manipualtion in a processor comprises the step of loading to a first register a first quadword from a memory using a first unaligned byte address. The unaligned byte address is the address of the first byte of a data item of N bytes being modified to remove low order three bits before applying to the memory whereby an aligned quadword is loaded to the first register. The loading to a second register a second quadword from the memory using a second unaligned byte address, which is the address of the first byte plus N-1, with the second unaligned byte address being modified to remove low order three bits before applying to the memory whereby an aligned quadword is loaded to the second register.

Next extracting a first part fo the data item from the first register by right shifting the content of the first register by a number of bytes corresponding to the value of the low order three bits of the unaligned byte address and zeroing the high order vacacted bits.

ADVANTAGE - Accomplishes all performance advantages of RISC type processor architecture, yet allows data structures and code previously generated for existing CISC type processors to be translated for use in high performance processor. @(36pp Dwg.No.1/11)@

Equivalent Alerting Abstract US A

The method of byte manipulation in the processor involves loading from a memory to a first register in the processor a first quad-word, the memory being addressed using a first unaligned byte address which is applied to the memory by the processor, the first unaligned byte address addressing a lowest-order first byte of a data item of N bytes, where N is an integer of variable size. The first unaligned byte address is modified to replace a lowest-order three bits of the first unaligned byte address with zeros before applying to the memory to address the first quad-word which is an aligned quad-word that is received by the processor from the memory and loaded to the first register. The lowest-order three bits of the first unaligned byte address is saved as a first shift amount.

The method also involves loading from the memory to a second register in the processor a second quad-word, the memory being addressed using a second unaligned byte address which is applied to the memory by the processor. The second unaligned byte address is the address of the first byte of the second quad-word plus N-1. The second unaligned byte address is modified to replace lowest-order three bits of the second unaligned byte address with zeros before applying to the memory to address the second quad-word which

is an aligned quad-word that is received by the processor from the memory
and loaded to the second register. The lowest-order three bits of the second unaligned byte address is saved as a second shift amount. First and
second parts of the data item are then selected and combined in one register.

ADVANTAGE - Accomplishes all performance advantages of RISC-type processor architecture, but allows data structures and code previously generated for existing CISC-type processors to be translated for use in high performance processor.

Equivalent Alerting Abstract US A

The byte operation method in a processor, involves loading to an internal
register a content of a selected memory location, the registers of N bytes,
the content containing an unaligned byte reference of M bytes in size where
M is any integer no more than N, the register and the selected memory location being addressed by an unaligned address to the unaligned byte reference but the content being aligned in the multiple-byte format. The
loading step is performed by a single instruction executed by the processor
performing in the processor an operation on the content, the operation changing only the unaligned byte reference in the internal register.

The content of the internal register is then stored to the selected memory location aligned in multiple-byte format using the unaligned address. The operation step includes extracting the unaligned byte reference from the content of the internal register, performing an arithmetic or logic operation on the extracted unaligned byte reference to
produce a result, then inserting the result into the content of the internal register at the unaligned byte reference before the step of storing.

USE/ADVANTAGE - Allows data structure and code for CISC processors to be
translated to RISC-y processor.

Title Terms/Index Terms/Additional Words: REGISTER; DATA; MANIPULATE; PROCESSOR; PERMIT; SIMPLIFY; MEMORY; ACCESS; WIDTH; ADDRESS; MODE; SET;
LIMIT; OPERATE

Class Codes

International Classification (Main): G06F-012/04, G06F-003/00, G06F-009/00,
G06F-009/30, G06F-009/308
(Additional/Secondary): G06F-012/00, G06F-015/76, G06F-009/31,
G06F-009/312, G06F-009/315
US Classification, Issued: 395800000, 395425000, 364232230, 364252500,
364252600, 364255100, 364259500, 364259700, 364DIG001, 395800000,
395400000, 395425000, 364232230, 364252600, 364255100, 364DIG001

File Segment: EPI;
DWPI Class: T01

Manual Codes (EPI/S-X): T01-F03B; T01-M04

Original Titles:
...In-register data manipulation using data **shift** in reduced **instruction**
set processor...

...In-register data manipulation for unaligned byte write using data **shift**
in reduced **instruction** set processor

Original Publication Data by Authority

Original Abstracts:
...byte extract, insert and masking, along with non-aligned load and store
instructions. The provision **of** load/locked and **store / conditional**
instructions permits **the** **implementation** of atomic byte writes. By
providing a conditional move instruction, many short branches can be...
...masking, along with non-aligned load and store instructions. The
provision of load/locked and **store / conditional** instructions permits the
implementation of atomic byte **writes** .

...

...masking, along with non-aligned load and store instructions. The
provision of load/locked and **store / conditional** instructions permits the
implementation **of** atomic byte writes.
Claims:
...by said right shifting;</br> extracting by said processor a second
part of said data item **from** said **second** register by left shifting the
content of the second register by a number of bytes e...

23/69,K/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005787330 - Drawing available
WPI ACC NO: 1992-009536/199202
XRPX Acc No: N1992-007331
Branching in pipelined processor - decodes instructions before executing
instructions to ensure optimal performance of code
Patent Assignee: COMPAQ COMPUTER CORP (COPQ); DIGITAL EQUIP CORP (DIGI)
Inventor: SITES R L; WITEK R T
Patent Family (8 patents, 6 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 463977	A	19920102	EP 1991401783	A	19910628	199202	B
CA 2045791	A	19911230				199213	E
TW 198109	A	19930111	TW 1991106670	A	19910822	199325	E
EP 463977	A3	19930922	EP 1991401783	A	19910628	199509	E
EP 463977	B1	19980729	EP 1991401783	A	19910628	199834	E
DE 69129881	E	19980903	DE 69129881	A	19910628	199841	E
			EP 1991401783	A	19910628		
KR 190252	B1	19990601	KR 199110880	A	19910628	200056	E
US 6167509	A	20001226	US 1990547629	A	19900629	200103	E
			US 1994243559	A	19940516		

Priority Applications (no., kind, date): US 1994243559 A 19940516; US 1990547629 A 19900629

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 463977	A	EN			
Regional Designated States,Original: DE FR GB NL					
CA 2045791	A	EN			
TW 198109	A	ZH			
EP 463977	A3	EN			
EP 463977	B1	EN			
Regional Designated States,Original: DE FR GB NL					
DE 69129881	E	DE			Application EP 1991401783 Based on OPI patent EP 463977
US 6167509	A	EN			Continuation of application US 1990547629

Alerting Abstract EP A

A pipelined processor is operated by fetching instructions from sequential addresses in memory and decoding the instructions before executing the instructions. The jump instructions are detected in the fetched instructions and the address of a register containing the address
of the target of the jump instruction is extracted.

A predicted target address is also extracted from the register. An instruction is prefetched from the predicted target address rather than from the sequential addresses before the jump instruction is executed.

USE/ADVANTAGE - High performance processors executing a reduced instruction set. The processor employs a variable memory page size so that
the entries in a translation buffer for implementing virtual addressing

can
be optimally used. @(34pp Dwg.No.1/11)@

Title Terms/Index Terms/Additional Words: BRANCH; PIPE; PROCESSOR; DECODE;
INSTRUCTION; EXECUTE; ENSURE; OPTIMUM; PERFORMANCE; CODE

Class Codes
International Classification (Main): G06F-009/00, G06F-009/38
US Classification, Issued: 712237000, 712205000, 712238000, 712239000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B; T01-H03A; T01-M04

Original Publication Data by Authority

Original Abstracts:
...byte extract, insert and masking, along with non-aligned load and store
instructions. The provision **of** load/locked and **store / conditional** instructions permits **the implementation** of atomic byte writes. By providing a conditional move instruction, many short branches can be...
Claims:
...an opcode, a register specifier and a memory address specifier, and extracting from said register **specifier** of **said** jump instruction an identification of a first of said registers for storing a first address which is a target address of said jump instruction, and extracting from said memory address **specifier** of **said** jump instruction a second address
which is a prediction of said target address; and prefetching...
?

33/69,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009715254
WPI ACC NO: 1999-631855/199954
XRPX Acc No: N1999-466430
Mask and shift instructions for ATM-type frame - Using logical OR operation on result for destination register
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
RD 422110	A	19990610	RD 1999422110	A	19990520	199954 B

Priority Applications (no., kind, date): RD 1999422110 A 19990520

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
RD 422110	A	EN	2	0	

Alerting Abstract RD A

NOVELTY - Instructions are MASH (mask and shift) and MASHO (mask and shift or). The MASH instruction takes five parameters - source register to get data from, most and least significant number of data to **keep** , shift **direction** and number of bits to shift the selected bit field. The MASHO instruction takes an additional parameter **specifying** the destination **register** . The result of the mask and shift operation is logically or-ed into the destination register, useful when multiple non-contiguous fields need to be concatenated.

USE - Instructions are for ATM or other network frames where the header has to be examined to determine which connection the frame is for.

ADVANTAGE - Instructions simplify the field extraction process.

Title Terms/Index Terms/Additional Words: MASK; SHIFT; INSTRUCTION; ATM; TYPE; FRAME; LOGIC; OPERATE; RESULT; DESTINATION; REGISTER

Class Codes
International Classification (Main): H04L

Mask and shift instructions for ATM-type frame...

Alerting Abstract ...parameters - source register to get data from, most and least significant number of data to **keep** , shift **direction** and number of bits to shift the selected bit field. The MASHO instruction takes an additional parameter **specifying** the destination **register** . The result of the mask and shift operation is logically or-ed into the

destination...

33/69,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006274883 - Drawing available
WPI ACC NO: 1993-067412/199308
XRPX Acc No: N1993-051665
Computer instruction executing appts. with pipelined architecture - sends instructions to executing unit according to logical sequence and shifts other instructions into vacant decoders
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: TRAN T M
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5185868	A	19930209	US 1990464918	A	19900116	199308 B

Priority Applications (no., kind, date): US 1990464918 A 19900116

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5185868	A	EN	8	3	

Alerting Abstract US A
The instruction executing apparatus executes instructions in a logical sequence according to a control program. An instruction buffer of FIFO construction serially is connected to a decoder buffer also of a FIFO construction. The decoder buffer includes a number of decoder units arranged in a hierarchical manner from a lowest-significance decoder unit to a highest-significance decoder unit in order to maintain the logical sequence of the instructions. The decoder units concurrently decode instructions transmitted from the instruction buffer and concurrently determine whether a corresponding decoded instruction is ready to be sent to an instruction executing unit.
Each decoder unit sends a corresponding instruction to the instruction executing unit. Instructions ready to be sent are sent to the instruction executing unit, according to the logical sequence. Instructions not ready to be sent are shifted to higher-significance available vacant decoder units, while maintaining the logical sequence of the instructions.
ADVANTAGE - High frequency operation. Efficient use of functional units.

Title Terms/Index Terms/Additional Words: COMPUTER; INSTRUCTION; EXECUTE;
APPARATUS; PIPE; ARCHITECTURE; SEND; UNIT; ACCORD; LOGIC; SEQUENCE; SHIFT
; VACANCY; DECODE

Class Codes
International Classification (Main): G06F-009/30
(Additional/Secondary): G06F-009/34, G06F-009/38
US Classification, Issued: 395375000, 364965400, 364965700, 364966200, 364DIG002, 364244300, 364244500

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-D02; T01-F03B

...**sends instructions to executing unit according to logical sequence and**
shifts other instructions into vacant decoders

Original Titles:
Apparatus having hierarchically arranged decoders concurrently decoding instructions and **shifting instructions** not ready for execution to vacant decoders higher in the hierarchy

Original Publication Data by Authority

Claims:
...certain conditions are satisfied, said certain conditions being source
operands necessary for execution of a **respective decoded instruction**
being available for delivery to said instruction execution means and said storage register means being available to receive resultant operands
of said **respective decoded instruction , each of** said plurality of
decoder units obtaining source operands when available from said storage
register means...

...one of said decoder units determines that said certain conditions are
not satisfied, shifting said **respective decoded instruction to a**
higher-significance available vacant decoder unit, maintaining said predetermined sequence and providing a corresponding decoded...

33/69,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005788180 - Drawing available
WPI ACC NO: 1992-010489/199202
XRPX Acc No: N1992-008049
In-register data manipulation in RISC processor - permitting only simplified memory access data width and addressing modes with set limited to register operations
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: SITES R; SITES R L; WITEK R; WITEK R T
Patent Family (10 patents, 7 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 465322	A	19920108	EP 1991401770	A	19910627	199202	B
CA 2045705	A	19911230				199213	E
EP 465322	A3	19921119	EP 1991401770	A	19910627	199342	E
US 5367705	A	19941122	US 1990547619	A	19900629	199501	E
			US 1993117482	A	19930907		
US 5410682	A	19950425	US 1990547619	A	19900629	199522	E
			US 1993117482	A	19930907		
			US 1994289025	A	19940810		
TW 285729	A	19960911	TW 1991106677	A	19910822	199704	E
EP 465322	B1	19990922	EP 1991401770	A	19910627	199943	E
DE 69131637	E	19991028	DE 69131637	A	19910627	199951	E
			EP 1991401770	A	19910627		
JP 3105960	B2	20001106	JP 1991254082	A	19910628	200059	E
KR 231380	B1	19991115	KR 199110879	A	19910628	200111	E

Priority Applications (no., kind, date): US 1994289025 A 19940810; US 1993117482 A 19930907; US 1990547619 A 19900629

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 465322	A	EN			
Regional Designated States,Original: DE FR GB NL					
CA 2045705	A	EN			
EP 465322	A3	EN			
US 5367705	A	EN	22	11	Continuation of application US 1990547619
US 5410682	A	EN	22	11	Continuation of application US 1990547619
					Continuation of application US 1993117482
					Continuation of patent US 5367705
TW 285729	A	ZH			
EP 465322	B1	EN			
Regional Designated States,Original: DE FR GB NL					
DE 69131637	E	DE			Application EP 1991401770
					Based on OPI patent EP 465322
JP 3105960	B2	JA	32		Previously issued patent JP 06119166

Alerting Abstract EP A

The method of byte manipualtion in a processor comprises the step of loading to a first register a first quadword from a memory using a first unaligned byte address. The unaligned byte address is the address of the first byte of a data item of N bytes being modified to remove low order three bits before applying to the memory whereby an aligned quadword is loaded to the first register. The loading to a second register a second quadword from the memory using a second unaligned byte address, which is the address of the first byte plus N-1, with the second unaligned byte address being modified to remove low order three bits before applying to the memory whereby an aligned quadword is loaded to the second register.

Next extracting a first part fo the data item from the first register by right shifting the content of the first register by a number of bytes corresponding to the value of the low order three bits of the unaligned byte address and zeroing the high order vacacted bits.

ADVANTAGE - Accomplishes all performance advantages of RISC type processor architecture, yet allows data structures and code previously generated for existing CISC type processors to be translated for use in high performance processor. @(36pp Dwg.No.1/11)@

Equivalent Alerting Abstract US A

The method of byte manipulation in the processor involves loading from a memory to a first register in the processor a first quad-word, the memory being addressed using a first unaligned byte address which is applied to the memory by the processor, the first unaligned byte address addressing a lowest-order first byte of a data item of N bytes, where N is an integer of variable size. The first unaligned byte address is modified to replace a lowest-order three bits of the first unaligned byte address with zeros before applying to the memory to address the first quad-word which is an aligned quad-word that is received by the processor from the memory and loaded to the first register. The lowest-order three bits of the first unaligned byte address is saved as a first shift amount.

The method also involves loading from the memory to a second register in the processor a second quad-word, the memory being addressed using a second unaligned byte address which is applied to the memory by the processor. The second unaligned byte address is the address of the first byte of the second quad-word plus N-1. The second unaligned byte address is modified to replace lowest-order three bits of the second unaligned byte address with zeros before applying to the memory to address the second quad-word

which
is an aligned quad-word that is received by the processor from the memory
and loaded to the second register. The lowest-order three bits of the second unaligned byte address is saved as a second shift amount. First and
second parts of the data item are then selected and combined in one register.

ADVANTAGE - Accomplishes all performance advantages of RISC-type processor architecture, but allows data structures and code previously generated for existing CISC-type processors to be translated for use in high performance processor.

Equivalent Alerting Abstract US A

The byte operation method in a processor, involves loading to an internal
register a content of a selected memory location, the registers of N bytes,
the content containing an unaligned byte reference of M bytes in size where
M is any integer no more than N, the register and the selected memory location being addressed by an unaligned address to the unaligned byte reference but the content being aligned in the multiple-byte format. The
loading step is performed by a single instruction executed by the processor
performing in the processor an operation on the content, the operation changing only the unaligned byte reference in the internal register.

The content of the internal register is then stored to the selected memory location aligned in multiple-byte format using the unaligned address. The operation step includes extracting the unaligned byte reference from the content of the internal register, performing an arithmetic or logic operation on the extracted unaligned byte reference to
produce a result, then inserting the result into the content of the internal register at the unaligned byte reference before the step of storing.

USE/ADVANTAGE - Allows data structure and code for CISC processors to be
translated to RISC-y processor.

Title Terms/Index Terms/Additional Words: REGISTER; DATA; MANIPULATE; PROCESSOR; PERMIT; SIMPLIFY; MEMORY; ACCESS; WIDTH; ADDRESS; MODE; SET;
LIMIT; OPERATE

Class Codes
International Classification (Main): G06F-012/04, G06F-003/00, G06F-009/00,
G06F-009/30, G06F-009/308
(Additional/Secondary): G06F-012/00, G06F-015/76, G06F-009/31,
G06F-009/312, G06F-009/315
US Classification, Issued: 395800000, 395425000, 364232230, 364252500,
364252600, 364255100, 364259500, 364259700, 364DIG001, 395800000,
395400000, 395425000, 364232230, 364252600, 364255100, 364DIG001

File Segment: EPI;

DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B; T01-M04

Original Titles:
...In-register data manipulation using data **shift** in reduced **instruction**
set processor...

...In-register data manipulation for unaligned byte write using data **shift**
in reduced **instruction** set processor

Original Publication Data by Authority

Original Abstracts:
...byte extract, insert and masking, along with non-aligned load and store
instructions. The provision **of** load/locked and **store / conditional**
instructions permits **the** **implementation** of atomic byte writes. By
providing a conditional move instruction, many short branches can be...
...masking, along with non-aligned load and store instructions. The
provision of load/locked and **store / conditional** instructions permits the
implementation of atomic byte **writes** .

...

...masking, along with non-aligned load and store instructions. The
provision of load/locked and **store / conditional** instructions permits the
implementation **of** atomic byte writes.
Claims:
...by said right shifting;</br> extracting by said processor a second
part of said data item **from** said **second** register by left shifting the
content of the second register by a number of bytes e...
?

36/69,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0015728560 - Drawing available
WPI ACC NO: 2006-290450/200630
Related WPI Acc No: 2001-376794; 2001-376796; 2001-383384; 2001-467003; 2001-467004; 2001-546627; 2002-165712; 2002-165714; 2003-089239; 2003-729705; 2004-459740; 2004-532453; 2005-055725; 2005-381287
XRPX Acc No: N2006-247399

Digital signal processor for cellular telephone, comprises microprocessor with instruction execution pipeline with pipeline phases, comprising program fetch circuitry , instruction decode circuitry, and at least one functional unit

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: HOYLE D; MARKANDEY V; NARDINI L

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20050188182	A1	20050825	US 1999173761	P	19991230	200630 B
			US 2000183527	P	20000218	
			US 2000702405	A	20001031	
			US 2005114549	A	20050426	

Priority Applications (no., kind, date): US 2000702405 A 20001031; US 2000183527 P 20000218; US 1999173761 P 19991230; US 2005114549 A 20050426

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20050188182	A1	EN	24	8	Related to Provisional US 1999173761
					Related to Provisional US 2000183527
					Division of application US 2000702405

Alerting Abstract US A1

NOVELTY - A digital system comprises a microprocessor with an instruction execution pipeline with pipeline phases, comprising program **fetch circuitry** that performs a first portion of the pipeline phases; instruction decode circuitry connected to receive fetched instructions from the program **fetch circuitry** ; and at least a first functional unit connected to receive control signals from the instruction decode circuitry.

DESCRIPTION - A digital system comprises a microprocessor having an instruction execution pipeline with pipeline phases. The microprocessor comprises program **fetch circuitry** that performs a first portion of the pipeline phases; instruction decode circuitry connected to receive fetched instructions from the program **fetch circuitry** , the instruction

decode
circuitry performs a second portion of the pipeline phases; and at least a
first functional unit connected to receive control signals (734) from the
instruction decode circuitry, with the functional unit performing a third
portion of the pipeline phases, the third portion being execution phases.
The first functional unit comprises byte intermingling circuitry (702)
connected to receive a single source operand having an ordered fields and
having outputs connected to provide a destination operand in response to
the control signals, where the byte intermingling circuitry is operable,
responsive to one of byte intermingling instructions, to place data from a
first selected field of the single source operand in a lower field of a
most significant portion of the destination operand, filling the remainder
of the most significant portion of the destination operand with zeroes, and
to place data from a second selected field of the single source operand,
the second selected field being contiguous with and less significant than
the first selected field, in a lower field of a least significant portion
of the destination operand, filling the remainder of the least significant
portion of the destination operand with zeroes. An INDEPENDENT CLAIM is
included for a method of operating a digital system having a microprocessor
and a set of byte intermingling instructions, comprising fetching a byte
intermingling instruction for execution; fetching a single source operand
selected by the byte intermingling instruction, the single source operand
comprising an ordered plurality of fields; and writing, into a lower field
of a most significant portion of a destination operand, data from a first
selected field of the single source operand and filling the remainder of
the most significant portion of the destination operand with zeroes, and
writing, into a lower field of a least significant portion of the
destination operand, data from a second selected field of the single source
operand, with the second selected field being contiguous with and less
significant than the first selected field, and filling the remainder of the
least significant portion of the destination operand with zeroes, with the
data selected in accordance with the byte intermingling instruction.

USE - Digital signal processor for a cellular telephone (claimed).

ADVANTAGE - The inventive digital system has microprocessors optimized for digital signal processing. It also has a processor having an improved instruction set architecture. The processor is code-compatible with C62xx DSP processors. It provides a superset of the C62x architecture while providing complete code compatibility for existing C62x code. The processor provides extensions to the existing C62x architecture in several areas: register file enhancements, data path extensions, additional functional unit hardware, increased orthogonality of the instruction set, data flow enhancements, 8-bit and 16-bit extensions, and additional instructions that reduce code size and increase register flexibility. It also has a set of multi-field byte intermingling instructions that provides features of single instruction, multiple data (SIMD) operation, reducing the code size and improving performance.

DESCRIPTION OF DRAWINGS - The figure is a more detailed block diagram of the intermingling circuit.

702 Intermingling circuitry
732 Mux control circuitry
734 Signals
src1, src2 Source operand

Technology Focus

ELECTRONICS - Preferred Function: The byte intermingling circuitry receives the single source operand and provides the destination operand during a single pipeline execution phase. Preferred System: The digital system further comprises a register file connected to the first functional unit for providing the single source operand and connected to the first functional unit to receive the destination operand; an integrated keyboard connected to the microprocessor via a keyboard adapter; a display, connected to the microprocessor via a display adapter; radio frequency (RF) circuitry connected to the microprocessor; and an aerial connected to the RF circuitry. Preferred Component: Each of the set of byte intermingling instructions has a field for identifying a predicate register. The first selected field is a most significant byte of the single source operand or is a second least significant byte of the single source operand. The second selected field is a next most significant byte of the single source operand; or is a least significant byte of the single source operand (src1, src2). Preferred Method: The step of writing is performed during a single

execution phase of the microprocessor.

Title Terms/Index Terms/Additional Words: DIGITAL; SIGNAL; PROCESSOR; CELLULAR; TELEPHONE; COMPRISE; MICROPROCESSOR; INSTRUCTION; EXECUTE; PIPE ; PHASE; PROGRAM; FETCH; CIRCUIT; DECODE; ONE; FUNCTION; UNIT

Class Codes
International Classification (Main): G06F-015/00
US Classification, Issued: 712224000

File Segment: EPI;
DWPI Class: T01; U21; W01
Manual Codes (EPI/S-X): T01-F03B1; T01-F03C; T01-J08A2; U21-A05D; W01-C01D3C

...**processor for cellular telephone, comprises microprocessor with instruction execution pipeline with pipeline phases, comprising program** fetch circuitry , **instruction decode circuitry, and at least one functional unit**

Alerting Abstract ...digital system comprises a microprocessor with an instruction execution pipeline with pipeline phases, comprising program **fetch circuitry** that performs a first portion of the pipeline phases; instruction decode circuitry connected to receive fetched instructions from the program **fetch circuitry** ; and at least a first functional unit connected to receive control signals from the instruction... ...comprises a microprocessor having an instruction execution pipeline with pipeline phases. The microprocessor comprises program **fetch circuitry** that performs a first portion of the pipeline phases; instruction decode circuitry connected to receive fetched instructions from the program **fetch circuitry** , the instruction decode circuitry performs a second portion of the pipeline phases; and at least...

Original Publication Data by Authority

Original Abstracts:
...of byte intermingling instructions. An instruction is provided that performs a shift right and byte **merge** operation. Another **instruction** is provided that performs a shift left and byte **merge** operation. Another **instruction** is provided that perform a byte swap operation. A set of instructions are provided that...
Claims:
...an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:program **fetch circuitry** operable

to perform a first portion of the plurality of pipeline phases;instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry , the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; andat least a first functional unit...

36/69,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0014520661 - Drawing available
WPI ACC NO: 2004-702607/200469
XRPX Acc No: N2004-557252
Personal computer in data processing system, has decoder that tracks position of program instructions within block of called program instructions and stores block counter value in block counter register accordingly
Patent Assignee: ARM LTD (ARMA-N)
Inventor: ELWOOD M P; VASEKIN V
Patent Family (7 patents, 106 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
GB 2400198	A	20041006	GB 20037821	A	20030404	200469	B
US 20040199754	A1	20041007	US 2004755449	A	20040113	200469	E
WO 2004088504	A1	20041014	WO 2003GB5388	A	20031211	200469	E
AU 2003292401	A1	20041025	AU 2003292401	A	20031211	200506	E
US 20050257037	A1	20051117	US 2004755449	A	20040113	200576	E
			US 2005121184	A	20050504		
GB 2400198	B	20060405				200624	E
TW 200421174	A	20041016	TW 2004100171	A	20040105	200648	E

Priority Applications (no., kind, date): GB 20037821 A 20030404

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
GB 2400198	A	EN	21	5	
WO 2004088504	A1	EN			

National Designated States,Original: AE AG AL AM AT AU AZ BA BB BG BR BW
BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR
HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW
MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT
TZ UA UG UZ VC VN YU ZA ZM ZW
Regional Designated States,Original: AT BE BG BW CH CY CZ DE DK EA EE ES
FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL
SZ TR TZ UG ZM ZW

AU 2003292401	A1	EN	Based on OPI patent	WO 2004088504
US 20050257037	A1	EN	C-I-P of application	US 2004755449
TW 200421174	A	ZH		

Alerting Abstract GB A
NOVELTY - A decoder controls data processing operations specified by program instructions fetched from a memory. The decoder tracks the position
of program instructions within the block of called program instructions and
stores block counter value in block counter register (22) accordingly.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

1.data processing method; and

2.computer program product including data processing program.

USE - For controlling execution of block of program instructions within
data processing system.
ADVANTAGE - Since location of program instructions is specified in different ways by using an offset field, the program instructions can be
easily located within block of program instructions.
DESCRIPTION OF DRAWINGS - The figures show the block diagram of computer
and call by execute block instruction data processing apparatus.
2 personal computer
22 block counter register

Title Terms/Index Terms/Additional Words: PERSON; COMPUTER; DATA; PROCESS;
SYSTEM; DECODE; TRACK; POSITION; PROGRAM; INSTRUCTION; BLOCK; CALL; STORAGE; COUNTER; VALUE; REGISTER; ACCORD

Class Codes
International Classification (Main): G06F-009/30
International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
G06F-0009/32	A	I R	R	20060101
G06F-0009/32	A	I L	B	20060101
G06F-0009/42	A	I F	B	20060101
G06F-0009/32	C	I R	R	20060101
G06F-0009/40	C	I F	B	20060101

US Classification, Issued: 712242000, 712242000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03C; T01-S03

Original Publication Data by Authority

Original Abstracts:
...A data processing apparatus and method are disclosed. The data processing apparatus comprises: an instruction **fetching circuit** operable to **fetch** a sequence of program instructions from a sequence of
memory locations; an instruction decoder **responsive to** program instructions **within** the sequence of program instructions fetched by the
instruction **fetching circuit** to **control data** processing operations
specified by the program instructions; and an execution **circuit** operable
under control **of the instruction decoder** to execute the **data** processing operations, wherein **the instruction decoder** is responsive
to an execute block instruction within the sequence of program instructions

to trigger fetching of a block of two or more program instructions by the instruction **fetching circuit** and execution of the block of two or more program instructions by the execution **circuit** , the block **of two** or more instructions containing a number of program instructions specified by a block length field...

...block of two or more program instructions is being processed to provide to the instruction **fetching circuit** the indication of the memory location of the instruction following the execute block instruction so that the **instruction following** the execute block instruction is fetched for execution immediately following the last instruction in the...

...of the memory location of the instruction following the execute block instruction to the instruction **fetching circuit** causes the **fetch** unit to fetch that instruction so that the correct sequence of instructions is **fetched by the fetch** unit **which** avoids the need to flush instructions...
...de programme a ete atteinte, un retour au deroulement du programme principal est declenche. Le **decodeur** d' **instructions** (14) peut **comprendre** un registre de compteur de bloc (22) pour suivre la position dans le bloc d...
Claims:
1. Apparatus for processing data, said apparatus comprising:an instruction **fetching circuit** operable to **fetch** program **instructions** **from** a sequence **of** memory locations;an instruction decoder responsive to program instructions fetched by said instruction **fetching circuit** to control **data** processing operations specified **by said** program instructions; andan execution **circuit** operable under control **of** said **instruction decoder** to execute said data processing operations; whereinsaid instruction decoder is responsive to an execute...

...instruction to trigger fetching of a block of two or more program instructions by said **instruction fetching circuit** and execution of said block of two or more program **instructions by** said execution circuit, said block of two or more instructions containing a number of program...

...1. A data processing apparatus comprising:an instruction **fetching circuit** operable to **fetch** a sequence of program instructions from a sequence of memory locations;an instruction decoder responsive

to
program instructions within said sequence of program instructions
fetched by said instruction fetching circuit to control data
processing
operations specified by said program instructions ; andan
execution
circuit operable under control of said instruction decoder to execute
said data processing operations, wherein said instruction decoder
is
responsive to an execute block instruction within said sequence of
program instructions to trigger fetching of a block of two or more
program
instructions by said instruction fetching circuit and execution of
said
block of two or more program instructions by said execution circuit
,
said block of two or more instructions containing a number of
program
instructions specified by a block length field within said executed
block
instruction and being...

...block of two or more program instructions is being processed to
provide
to said instruction fetching circuit said indication of said memory
location of said instruction following said execute block instruction
so
that said instruction following said execute block instruction is
fetched
for execution immediately following said last instruction in said
block
of two or more program instructions.

36/69,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0014344264 - Drawing available
WPI ACC NO: 2004-532453/200451
Related WPI Acc No: 2001-376794; 2001-376796; 2001-383384; 2001-467003; 2001-467004; 2001-546627; 2002-165712; 2002-165714; 2003-089239; 2003-729705; 2004-459740; 2005-055725; 2005-381287; 2006-290450
XRPX Acc No: N2004-421637

Digital signal processor shifts source operand and signed shift count value in response to control signals from instruction decoding circuit during single pipeline execution phase

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: HOYLE D; SCALES R H; WANG M; ZBICIAK J R

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 6757819	B1	20040629	US 2000183527	P	20000218	200451 B
			US 2000703141	A	20001031	

Priority Applications (no., kind, date): US 2000183527 P 20000218; US 2000703141 A 20001031

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6757819	B1	EN	20	9	Related to Provisional US 2000183527

Alerting Abstract US B1

NOVELTY - A shift circuit shifts the source operand and a signed shift count value in response to control signals from instruction decoding circuit, and outputs a destination operand during a single pipeline execution phase.

DESCRIPTION - An INDEPENDENT CLAIM is also included for digital signal processor operating method.

USE - For digital signal processing.

ADVANTAGE - Optimizes digital signal processing.

DESCRIPTION OF DRAWINGS - The figure shows a block diagram of the digital signal processor.

Title Terms/Index Terms/Additional Words: DIGITAL; SIGNAL; PROCESSOR; SHIFT ; SOURCE; OPERAND; SIGN; COUNT; VALUE; RESPOND; CONTROL; INSTRUCTION; DECODE; CIRCUIT; SINGLE; PIPE; EXECUTE; PHASE

Class Codes
International Classification (Main): G06F-015/82
(Additional/Secondary): G06F-009/305, G06F-009/315
US Classification, Issued: 712300000, 712213000, 712223000, 708209000, 708233000, 708236000

File Segment: EPI;

DWPI Class: T01; U22
Manual Codes (EPI/S-X): T01-F03B1; U22-G05

Original Publication Data by Authority

Original Abstracts:
...data processing system is provided with a digital signal processor which
has an instruction for **shifting** a **source** operand in response to a signed shift count value and storing the shifted result in...

...to the shift count value and in a direction according to the sign of the
shift count. One **instruction** is provided that performs **a** right **shift**
for a positive shift count and a left shift for a negative shift count,
and another **instruction** is provided performs a left **shift** for **a** positive shift count and a right shift for a negative shift count. If the
shift...
Claims:
...an instruction execution pipeline with a plurality of pipeline phases,
wherein the microprocessor comprises:program **fetch** **circuitry** operable
to perform a first portion of **the** **plurality** of pipeline phases;instruction decode circuitry connected to receive fetched instructions from the program **fetch** **circuitry** , **the** instruction decode
circuitry **operable** to perform a second **portion** **of** the plurality of
pipeline phases; andat least a first functional unit connected to receive
...

...from the instruction decode circuitry, the signed shift count value including a sign and a **shift** count **value** , wherein for a first **shifting**
instruction the shift circuitry shifts the source operand right by the
shift count value **if** **the** sign is positive or left if the sign is negative onto the destination operand outputs, wherein for a second **shifting** **instruction** the shift circuitry shifts the source operand left
by the shift count value **if** **the** sign is positive or right if the sign
is negative onto the destination operand outputs...

...the first functional unit is operable to provide the shifted result in
response to the **shifting** **instructions**.>

36/69,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013244049 - Drawing available
WPI ACC NO: 2003-329220/200331
XRPX Acc No: N2003-263356
Data processing system for image processing, has general-purpose processing unit which operates in either one of two modes to perform operation on instruction obtained from fetch unit or special-purpose processing unit
Patent Assignee: PACIFIC DESIGN INC (PACI-N); PACIFIC DESIGN KK (PACI-N);
SATOU T (SATO-I)
Inventor: SATO T; SATOU T
Patent Family (5 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
US 20020199081	A1	20021226	US 2002175446	A	20020620	200331	B
GB 2380282	A	20030402	GB 200214388	A	20020621	200331	E
JP 2003005957	A	20030110	JP 2001191423	A	20010625	200331	E
GB 2380282	B	20050720	GB 200214388	A	20020621	200547	E
US 6948049	B2	20050920	US 2002175446	A	20020620	200562	E

Priority Applications (no., kind, date): US 2002175446 A 20020620; JP 2001191423 A 20010625
Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20020199081	A1	EN	17	7	
JP 2003005957	A	JA	13		

Alerting Abstract US A1
NOVELTY - A fetch unit respectively supplies instruction code fetched from memory to special-purpose processing unit (VU) or general-purpose processing unit (PU), on identifying the code to be special-purpose instruction or general-purpose instruction. The general-purpose processing
unit operates in either one of two modes to perform operation on instruction obtained from fetch unit or special-purpose processing unit.
DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

1.control method; and

2.computer readable recording medium storing data processing program.

USE - In data processing systems equipped with dedicated circuits. Also
used in data processor for image processing and network processing.
ADVANTAGE - Reduces overheads of data transfer between PU and VU without
sacrificing general-purpose nature of PU. Enables VU to process data without consuming larger number of clock cycles, which are consumed to data
transfer between PU and VU.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of data processing apparatus.

PU general-purpose processing unit
VU special-purpose processing unit

Title Terms/Index Terms/Additional Words: DATA; PROCESS; SYSTEM; IMAGE; GENERAL; PURPOSE; UNIT; OPERATE; ONE; TWO; MODE; PERFORMANCE; INSTRUCTION ; OBTAIN; FETCH; SPECIAL

Class Codes
International Classification (Main): G06F-015/00, G06F-009/38
(Additional/Secondary): G06F-009/30
US Classification, Issued: 712034000, 712043000, 712229000, 712034000, 712205000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-C04D; T01-M05; T01-S03

Original Publication Data by Authority

Claims:
...that specifies processing to be performed by the special-purpose processing unit, the special-purpose **instruction** **or** a **decoded** data of the special-purpose instruction to the special-purpose processing unit, and supplying, when...

...general-purpose instruction that specifies processing by the general-purpose processing unit, the general-purpose **instruction** or a **decoded** **data** of the general-purpose instruction to the general-purpose processing unit,wherein the general-purpose...

...a general-purpose processing unit that is suited to general-purpose data processing; anda **fetch** unit **for** supplying, when an instruction code fetched from a code memory is a special-purpose instruction...

36/69,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0011170350 - Drawing available
WPI ACC NO: 2002-107986/200215
XRPX Acc No: N2002-080414
Sub-pipelined translation structure has multiplexer selecting output from base and migrant decoders depending on fetch packet operation mode
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: SCHTAS D E; SIMA L R; SIMAR L R; STEISS D E
Patent Family (6 patents, 30 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 1168159	A1	20020102	EP 2001251	A	20010625	200215	B
JP 2002041283	A	20020208	JP 2001193066	A	20010626	200215	E
CN 1365047	A	20020821	CN 2001122080	A	20010614	200281	E
TW 518516	A	20030121	TW 2001115471	A	20010626	200356	E
US 6895494	B1	20050517	US 2000603226	A	20000626	200533	E
CN 1175348	C	20041110	CN 2001122080	A	20010614	200626	E

Priority Applications (no., kind, date): US 2000603226 A 20000626

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 1168159	A1	EN	10	3	

Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR
IE IT LI LT LU LV MC MK NL PT RO SE SI TR

JP 2002041283	A	JA	8		
TW 518516	A	ZH			

Alerting Abstract EP A1

NOVELTY - A shared data path parses the fetched instruction packets having base and migrant architecture modes, into corresponding execute packets. The base and migrant architecture instructions from the shared path are decoded by respective decoders, based on execution mode of instructions. The outputs of migrant and base decoders are selected by a multiplexer depending on the operating mode of fetch packet.

DESCRIPTION - An INDEPENDENT CLAIM is also included for binary compatibility provision method.

USE - Sub-pipelined translation structure for real time DSP applications.

ADVANTAGE - Allows rapid mode transition, since packets are assigned to different modes. Instruction graduation and instruction dependencies are not required, thus reducing complexity and hardware in instruction decoder.

DESCRIPTION OF DRAWINGS - The figure shows the sub-pipelined translation structure.

Title Terms/Index Terms/Additional Words: SUB; PIPE; TRANSLATION; STRUCTURE
; MULTIPLEX; SELECT; OUTPUT; BASE; DECODE; DEPEND; FETCH; PACKET;

OPERATE
; MODE

Class Codes
International Classification (Main): G06F-015/00, G06F-009/30, G06F-009/38
(Additional/Secondary): G06F-009/318
US Classification, Issued: 712024000, 712209000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B; T01-J08A2

Original Publication Data by Authority

Original Abstracts:
...migrant). The two execution modes have separate control logic. Instructions from the dispatch datapath are **decoded** by either **base** architecture **decode** logic or the migrant architecture decode logic, depending on the execution mode bound to the...
Claims:
...and a migrant architecture decode for decoding said base architecture
instructions and said migrant architecture **instructions** , **respectively** ,
in **dependence** upon the execution mode of the fetch packet of **the instructions** being **decoded** , prior to executing;a multiplexer having at
least two inputs and one machine word output...

...circuit for dispatching execute packet instructions having a base execution mode;a migrant architecture control **circuit** for **dispatching**
execute packet instructions having a migrant execution mode;a base architecture decode connected to said...

36/69,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010972218 - Drawing available
WPI ACC NO: 2001-596037/200167
XRPX Acc No: N2001-444289
Pre- decoding one-byte instruction prefixes and branch instruction indicators
Patent Assignee: INTEL CORP (ITLC)
Inventor: GRUNER F R; ZAVERI B
Patent Family (7 patents, 92 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 2001044929	A2	20010621	WO 2000US41327	A	20001019	200167	B
AU 200127459	A	20010625	AU 200127459	A	20001019	200167	E
GB 2373901	A	20021002	WO 2000US41327	A	20001019	200273	E
			GB 200215172	A	20020701		
US 6496923	B1	20021217	US 1999466534	A	19991217	200307	E
CN 1434937	A	20030806	CN 2000819062	A	20001019	200366	E
GB 2373901	B	20040714	WO 2000US41327	A	20001019	200446	E
			GB 200215172	A	20001019		
CN 1186719	C	20050126	CN 2000819062	A	20001019	200620	E

Priority Applications (no., kind, date): US 1999466534 A 19991217

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 2001044929	A2	EN	26	7	

National Designated States,Original: AE AG AL AM AT AU AZ BA BB BG BR BY
BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN
IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ
PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH
GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW

AU 200127459	A	EN	Based on OPI patent WO 2001044929
GB 2373901	A	EN	PCT Application WO 2000US41327 Based on OPI patent WO 2001044929
GB 2373901	B	EN	PCT Application WO 2000US41327 Based on OPI patent WO 2001044929

Alerting Abstract WO A2

NOVELTY - A number of instruction indicators are generated. A prefix and branch decode unit (512) combines at least two of the instruction indicators. A prefix and branch decode unit combines at least two of the instruction indicators, and a pre-decode unit (56) decodes the combined instruction indicators. The one-byte branch and address size indicators are combined by logic OR to produce an address size or branch indicator.

DESCRIPTION - AN INDEPENDENT CLAIM is made for:

1.A system for pre- decoding one-byte instruction prefixes and branch instruction ;

2. Logic for pre- decoding one-byte instruction prefixes and branch instruction indicators.

USE - For **detecting** one-byte **prefixes** and branch type macro-**instructions** .

ADVANTAGE - Boundaries between instructions can be detected with relative ease. Decoding can be by multiplexing an address size or branch indicator with an opcode/prefix indicator and a code segment descriptor indicator to produce an address size. Address size or branch indicator is multiplexed with opcode or prefix indicator to produce a one-byte branch indicator (Claimed). Combined indicators are multiplexed with opcode/prefix indicator and a code segment descriptor (CSD) indicator to produce an address size, data size, or repeat indicator. In parallel with first multiplexing, combined indicators are multiplexed with opcode/prefix indicator and a branch for multiple prefix indicator to produce a one-byte branch indicator, an FF-two-byte branch indicator, or an OF-two-byte branch indicator.

DESCRIPTION OF DRAWINGS - Drawing shows a block diagram of one embodiment of an architecture of the instruction pre-decoder (IPD) according to present invention.

56 Instruction pre-decoder

512 Prefix and branch decode unit.

Title Terms/Index Terms/Additional Words: PRE; DECODE; ONE; BYTE; INSTRUCTION; BRANCH; INDICATE

Class Codes

International Classification (Main): G06F-009/30
(Additional/Secondary): G06F-009/318, G06F-009/38
US Classification, Issued: 712213000, 712210000, 712233000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03

Pre- decoding one-byte instruction prefixes and branch instruction indicators

Original Titles:

Length decode to **detect** one-byte **prefixes** and branch...
...LENGTH DECODE TO **DETECT** ONE-BYTE **PREFIXES** AND BRANCH...

...DECODAGE DE LONGUEUR POUR LA **DETECTION** DE **PREFIXES** D'UN OCTET ET DE BRANCHE

Alerting Abstract ...A system for pre- **decoding** one-byte

instruction
prefixes and branch **instruction** ; **Logic** for pre- **decoding** one-byte **instruction** **prefixes** and **branch** **instruction** indicators.
...

...USE - For **detecting** one-byte **prefixes** and branch type macro-**instructions** .

Original Publication Data by Authority

Original Abstracts:
The invention provides a system and method which can be used for pre-**decoding** one-byte **instruction** **prefixes** and branch **instruction** **indicators** . A static line **detect** generates a number **of** instruction indicators. Further, a **prefix** and branch **decode** **unit** combines at least two of the number of instruction indicators, and a **pre - decode** unit **decodes** the **combined** **instruction** **indicators** . Embodiments of
the invention **decode** one byte **prefixes** without additional cycle penalty and generate one and two byte branch indications early...

...A system and method for pre- **decoding** one-byte instruction **prefixes**
and branch **instruction** indicators **is** described. A **static** **line** **detect** generates a number of instruction indicators. Further, a **prefix**
and branch **decode** unit **combines** at least two **of** the number **of** **instruction** indicators, and a pre-decode unit decodes the combined instruction indicators...

...des prefixes d'instructions a un octet et des indicateurs d'instructions
de branches. Une **detection** de ligne statique genere un certain nombre d'indicateurs d'instructions. En outre, une unite...
Claims:
What is claimed is:1. A method comprising:pre- **decoding** branch and **instruction** **prefix** information;combining the branch **and** **instruction**
prefix **information** **into** a signal;sending bits to facilitate **decoding**
the **signal** ; and **decoding** the signal during an instruction decode phase
based on the bits to **detect** one-byte **prefix** and branch information without incurring additional cycle penalty.

36/69,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010762920 - Drawing available
WPI ACC NO: 2001-376794/200140
Related WPI Acc No: 2001-376796; 2001-383384; 2001-467003; 2001-467004; 2001-546627; 2002-165712; 2002-165714; 2003-089239; 2003-729705; 2004-459740; 2004-532453; 2005-055725; 2005-381287; 2006-290450
XRPX Acc No: N2001-275796

Complex multiplication circuit for digital signal processor used in cellular phones, produces product of most and least significant portions of source operands

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: AL J R Z E; BALMER K; BHANDAL A A S; BHANDAL A S; GOLSTON J E; GOSDEN J E; GUTTAG K M; HOYLE D; HULLEY D; HUSSAIN Z; MARKANDEY V; SIMAR L R; STEISS D E; STOTZER E J; ZBICIAK J R

Patent Family (10 patents, 30 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 1102161	A2	20010523	EP 2000310113	A	20001114	200140	B
JP 2001202245	A	20010727	JP 2000403992	A	20001115	200148	E
JP 2001256038	A	20010921	JP 2000348735	A	20001115	200170	E
CN 1309347	A	20010822	CN 2000133915	A	20001115	200175	E
US 6671797	B1	20031230	US 2000183527	P	20000218	200402	E
			US 2000702463	A	20001031		
TW 543000	A	20030721	TW 2000124170	A	20001115	200406	E
US 6711602	B1	20040323	US 2000183527	P	20000218	200421	E
			US 2000183654	P	20000218		
			US 2000703093	A	20001031		
US 6766440	B1	20040720	US 2000183527	P	20000218	200448	E
			US 2000702453	A	20001031		
CN 1194292	C	20050323	CN 2000133915	A	20001115	200634	E
US 7062526	B1	20060613	US 2000183527	P	20000218	200639	E
			US 2000183654	P	20000218		
			US 2000703140	A	20001031		

Priority Applications (no., kind, date): US 2000703140 A 20001031; US 2000703093 A 20001031; US 2000702463 A 20001031; US 2000702453 A 20001031; US 2000183527 P 20000218; US 1999165512 P 19991115; US 2000183654 P 20000218

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 1102161	A2	EN	48	22	
Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2001202245	A	JA	113		
JP 2001256038	A	JA	27		
US 6671797	B1	EN			Related to Provisional US 2000183527
TW 543000	A	ZH			
US 6711602	B1	EN			Related to Provisional US

2000183527
Related to Provisional US
2000183654
US 6766440 B1 EN Related to Provisional US
2000183527
US 7062526 B1 EN Related to Provisional US
2000183527
Related to Provisional US
2000183654

Alerting Abstract EP A2

NOVELTY - Multipliers (173a,173b) receive the most and least significant portions of different source operands respectively. Shifters produce shifted products of multipliers. An adder/converter (177) adds the shifted products to form a full precision product having a double width.

DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

1.Microprocessor with multiply circuit;

2.Digital system with microprocessor

USE - For digital signal processor used in electronic products such as high speed modems, digital cellular phones, complex automotive system, video conferencing equipment and for digital systems such as video phones, network processing natural speed interfaces, ultra high speed modems.

ADVANTAGE - Since the multipliers independently select the most and least significant portions of source operand for complex computation, a larger number of multiply functions are enabled and hence the performance of digital signal processing is improved. Also, the multiplied products are shifted to avoid overflow of bits.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of multiply unit group in processor.

173a,173b Multipliers

177 Adder/converter

Title Terms/Index Terms/Additional Words: COMPLEX; MULTIPLICATION; CIRCUIT; DIGITAL; SIGNAL; PROCESSOR; CELLULAR; TELEPHONE; PRODUCE; PRODUCT; SIGNIFICANT; PORTION; SOURCE; OPERAND

Class Codes

International Classification (Main): G06F-007/00, G06F-007/52, G06F-009/30, G06F-009/315, G06F-009/38

(Additional/Secondary): G06F-011/00, G06F-012/00, G06F-013/38, G06F-017/16, G06F-007/72, G06F-009/305

International Classification (+ Attributes)

IPC + Level Value Position Status Version

G06F-0007/38 A I L B 20060101
G06F-0007/52 A I F B 20060101
G06F-0007/48 C I F B 20060101
US Classification, Issued: 712224000, 712223000, 712213000, 712219000, 712214000, 712300000, 708625000, 712218000, 708620000, 708550000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-E02B; T01-E03; T01-J04C

Original Publication Data by Authority

Claims:
...an instruction execution pipeline with a plurality of pipeline phases,
wherein the microprocessor comprises:program **fetch circuitry** operable
to perform a first portion of the plurality of pipeline phases;instruction
decode circuitry connected to receive fetched instructions form **the program fetch circuitry** , the instruction decode circuitry operable to
perform a second portion of the plurality of pipeline phases; andat least a
first functional unit **connected to** receive a plurality of control signals from the instruction decode circuitry, the functional unit operable
...

...source and said second data source, said second multiplier circuit forming a second product of **an instruction** selected portion of said first data source and **an instruction** selected portion of said second
data source;a second shifter connected to said second multiplier...

...shift amount; andan arithmetic circuit connected to said first shifter
and to said second **shifter** forming an **instruction** selected arithmetic
combination of said first shifted product applied to most significant bits
and said

36/69,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009666424 - Drawing available
WPI ACC NO: 1999-619933/199953
XRPX Acc No: N1999-457222
Computer instruction supplying method for processor of computer system
Patent Assignee: SGS THOMSON MICROELTRN LTD (SGSA)
Inventor: CUMMING P; GRISENTHWAITE R
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5978908	A	19991102	US 1996735864	A	19961023	199953 B

Priority Applications (no., kind, date): GB 199521978 A 19951026

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5978908	A	EN	22	9	

Alerting Abstract US A

NOVELTY - A testing operation to locate branch instructions from fetched sequence of instructions is performed. Testing causes retrieval of new sequence of instruction from target address store for branch operation and makes branch instructions in the sequence prior to the initial instruction to be ignored.

DESCRIPTION - Several instructions to be executed by the processor are stored in a sequence in a storage unit at addressable locations. After testing the sequence of instructions that is fetched from the storage unit to locate a branch instruction which is predicted to be taken, branch operation is enabled. Interin updation of the branch prediction value of branch instruction is preformed prior to execution of branch instruction, and the interin update is corrected if actual execution of the branch instruction indicates that interin updated value is incorrect. The test operation is performed successively of any branch instructions in sequence from initial instruction, to test the probability of branch being taken, and disregards branch instructions in the sequence after initial branch instruction that is predicted is taken. An INDEPENDENT CLAIM is also included for circuit for supplying instruction to processor.

USE - For supplying instructions to processor of computer system.

ADVANTAGE - Complexity and size of devices is increased by increasing number of content addressable memory cell, thus reducing number of occasions on which a branch instruction needs to be written-in.

DESCRIPTION OF DRAWINGS - The figure shows content of CAM (content addressable memory) cells and data RAM's of branch target buffer.

Title Terms/Index Terms/Additional Words: COMPUTER; INSTRUCTION; SUPPLY;

METHOD; PROCESSOR; SYSTEM

Class Codes
International Classification (Main): G06F-009/38
US Classification, Issued: 712240000, 712238000, 712239000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B

Original Publication Data by Authority

Original Abstracts:
A computer instruction supply system has store and **fetch circuitry** for obtaining **a sequence** of instructions, test circuitry for locating the first instruction in the sequence to be enabled...
Claims:
...locations; fetching from said store a sequence of instructions for decoding and execution by the **processor** ; supplying **data** indicative of **each** instruction to **a** respective partition of a CAM array dependent on the position of the instruction in said...

36/69,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009571008 - Drawing available
WPI ACC NO: 1999-517903/199943
XRPX Acc No: N1999-385144
Variable length instruction processor with self timed marking for executing series of operations in computer systems
Patent Assignee: INTEL CORP (ITLC)
Inventor: BEEREL P A; GINOSAR R; KOL R; MYERS C J; ROTEM S; STEVENS K S; YUN K Y

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5948096	A	19990907	US 1997997462	A	19971223	199943 B

Priority Applications (no., kind, date): US 1997997462 A 19971223

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5948096	A	EN	13	5	

Alerting Abstract US A
NOVELTY - The marking unit (34) has a marking input and a pair of marking outputs. The marking outputs are directly coupled to their respective downstream marking units, to provide marking signal. The marking input is directly coupled to upstream marking unit to provide marking signal.
DESCRIPTION - A self timed length decoder (602) is coupled to a buffer, which receives bytes, and has one length output, one prefix output and one prefix input. A self timed marking unit (34) is connected to the length decoder (602) via prefix signal lines (604). An INDEPENDENT CLAIM is also included for a method of self timed marking of instructions.
USE - For executing series of operations in computer system.
ADVANTAGE - Since marking system uses prefixes to accommodate presence of bytes, proper length decoding and marking is performed.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of computer system with self timed marking circuit.
34 Marking unit
602 Self timed length decoder
604 Prefix signal lines

Title Terms/Index Terms/Additional Words: VARIABLE; LENGTH; INSTRUCTION; PROCESSOR; SELF; TIME; MARK; EXECUTE; SERIES; OPERATE; COMPUTER; SYSTEM

Class Codes

International Classification (Main): G06F-009/30
US Classification, Issued: 712210000, 712212000, 712213000, 712245000, 712246000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03

Original Publication Data by Authority

Original Abstracts:
...self-timed instruction marking circuit includes a prefix handling system
for processing instruction bytes having **prefix** **bytes** . Length **decoders**
receive **instruction** data **bytes** , and **perform** length **decoding** independently of the other length decoders in the instruction marking circuit. A length decoder determines whether a byte **being** processed is a
prefix byte to an instruction. If a length-affecting prefix byte is found,
the length decoder...

36/69,K/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009016396 - Drawing available
WPI ACC NO: 1998-573071/199849
XRPX Acc No: N1998-446243
Information processor - includes pipeline control circuit which forwards calculation result related to load instruction, to storage register
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: KUBOTA J
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
JP 10254698	A	19980925	JP 199759131	A	19970313	199849 B

Priority Applications (no., kind, date): JP 199759131 A 19970313

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 10254698	A	JA	5	4	

Alerting Abstract JP A
The processor includes an instruction **fetch circuit** (2) which reads instruction from an instruction memory in order from every stage. An instruction decoding circuit (3) **decodes** the read **instruction** in **specified** order by the instruction **fetch circuit** . An address decoding circuit calculates and decodes the address which is access from the decoded instruction. A calculation circuit performs the calculation by which instruction is performed from the decoded instruction. A pipeline processing type information processor is provided with the general purpose register which stores the data required for execution. The instruction circuit reads several instructions from the instruction memory. A load instruction search circuit searches load instruction.
An instruction coding circuit decodes the instruction corresponding to the next searched load instruction. An operand comparator circuit judges whether the execution stole occurs in the instruction. A load address calculation circuit calculates the address which is accessed by load instruction when being judged with the execution stole arising by the calculation circuit. A load instruction address holding circuit whose address of the load instruction that has been judged by the execution stole. An address comparator circuit compares the instruction address and the program count number shows the order of read-out to the instruction **fetch circuit** . A pipeline control circuit forward the calculation result to the storing register.
ADVANTAGE - Avoids producing pipeline delay. Features improved capacity.
Title Terms/Index Terms/Additional Words: INFORMATION; PROCESSOR; PIPE;

CONTROL; CIRCUIT; FORWARD; CALCULATE; RESULT; RELATED; LOAD; INSTRUCTION;
STORAGE; REGISTER

Class Codes
International Classification (Main): G06F-009/38

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B1

Alerting Abstract ...The processor includes an instruction **fetch circuit** (2) which reads instruction from an instruction memory in order from every stage. An instruction decoding circuit (3) **decodes** the read **instruction** in **specified** order by the instruction **fetch circuit** . An address decoding circuit calculates and decodes the address which is access from the decoded...

...address and the program count number shows the order of read-out to the instruction **fetch circuit** . A pipeline control circuit forward the calculation result to the storing register...

36/69,K/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008507869 - Drawing available
WPI ACC NO: 1998-038753/199804
XRPX Acc No: N1998-031225
4-bit up counter - has second counter part with shift circuit to receive carry signal from third latch circuit which receives carry signal from shift circuit of first counter part
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ); RENESAS TECHNOLOGY KK (RENE-N)
Inventor: MIURA H
Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
JP 9292973	A	19971111	JP 1996105596	A	19960425	199804	B
US 5754616	A	19980519	US 1996712626	A	19960911	199827	E
JP 3567309	B2	20040922	JP 1996105596	A	19960425	200462	E

Priority Applications (no., kind, date): JP 1996105596 A 19960425

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 9292973	A	JA	14	14	
JP 3567309	B2	JA	17		Previously issued patent JP 09292973

Alerting Abstract JP A

The counter includes first and second counter parts. The first counter part includes two pairs of latch circuits (1a,1b,2a,2b) and shift circuits (3a,3b). The first pair of latch circuits operate in synchronization with first clock and second pair of latch circuit operate in synchronization with second clock. The first latch circuit latches data applied, in synchronization with first clock. The latched data is shifted and latched into second latch circuit which operates in synchronization with second clock. The shift circuit outputs a carry signal. A similar circuit consisting a loop of latch and shift circuits performs a similar operation.

The first counter part counts the data of lower order bits based on first and second clock circuits.

A third latch circuit (4) accepts carry signal from the shift circuit of first counter part. The second counter part includes latch circuits (1c,1d,2c,2d) and shift circuits (3c,3d). The first latch circuits (1c,1d) latches data in synchronization with second clock pulse and the latched data is shifted. The second latch circuit (2c,2d) latches shifted data in synchronization with first clock pulse. The shift circuit outputs a

carry
signal. The second counter part counts the higher order bit of count value
based on first clock and second clock. The shift circuit in second counter
part receives the carry signal from the third latch circuit.
ADVANTAGE - Offers high speed counting.

Title Terms/Index Terms/Additional Words: BIT; UP; COUNTER; SECOND; PART;
SHIFT; CIRCUIT; RECEIVE; CARRY; SIGNAL; THIRD; LATCH; FIRST

Class Codes
International Classification (Main): G06F-007/00, H03K-021/16
US Classification, Issued: 377115000, 377043000, 377078000

File Segment: EPI;
DWPI Class: T01; U21
Manual Codes (EPI/S-X): T01-E02; U21-D03; U21-D05

Original Publication Data by Authority

Claims:
...a first latch circuit for latching data synchronously with a first clock; a first shift **circuit** for **fetching** data latched by the first **latch circuit and** outputting data shifted in response to a **shift instruction** data and outputting the **shift instruction data when** a predetermined **shift** operation **occurs** ; **and** a second latch circuit for latching data outputted by the first shift circuit synchronously with...

...a third latch circuit for latching data synchronously with the second clock; a second shift **circuit** for **fetching** data latched by the third latch circuit and outputting data shifted in response **to** a **shift instruction** data and outputting the **shift instruction** data when a predetermined shift operation occurs; and **a fourth** latch circuit for latching **data outputted** by the second shift circuit synchronously with the first clock, and latching the latched data...

...latch circuit to the third latch circuit; and a fifth latch circuit for latching the **shift instruction** data outputted from the first shift circuit and outputting the latched data from the fifth latch circuit to **the second** shift circuit; wherein the second latch circuit and the third latch circuit, respectively, obtain data...

36/69,K/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007027242 - Drawing available
WPI ACC NO: 1995-043738/199506
XRPX Acc No: N1995-034316
JTAG component instruction error detection - connecting JTAG serial test
bus boundary scan path to single bit bypass register when errors occur
Patent Assignee: AT & T GLOBAL INFORMATION SOLUTIONS CO (AMTT)
Inventor: SIMPSON D L; TAYLOR M A
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5377198	A	19941227	US 1991799507	A	19911127	199506 B

Priority Applications (no., kind, date): US 1991799507 A 19911127

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5377198	A	EN	32	26	

Alerting Abstract US A
The method for detecting errors in instructions used to control a serial test bus in a computer system involves setting up several components to connect instruction registers to receive instructions via the bus path. Instructions are **shifted** into the **instruction** registers and their validity checked. All the components containing valid instructions are set up to connect their boundary scan registers to receive data corresp. to the valid instructions via the bus path. Those components containing invalid instructions connect their bypass registers to the bus path.
Data to be shifted into the boundary scan registers is prefixed with a header as long as the longest boundary scan register in the bus path and having a predetermined number of LSBs equal to the same value. The data and header are shifted into the components. Signals shifted out of the components are received as the data and header are shifted into the components. A portion of the signals shifted out of the components which should correspond to the header is monitored to detect errors in the instructions used to control the test bus.
ADVANTAGE - Requires no component pins or connections in addition to normal connections required for standard JTAG operation.

Title Terms/Index Terms/Additional Words: COMPONENT; INSTRUCTION; ERROR;
DETECT; CONNECT; SERIAL; TEST; BUS; BOUNDARY; SCAN; PATH; SINGLE; BIT;
REGISTER; OCCUR

Class Codes
International Classification (Main): H04B-017/00
US Classification, Issued: 371022300

File Segment: EPI;
DWPI Class: S01; T01; U11; V04
Manual Codes (EPI/S-X): S01-G01A1; T01-G02A2; U11-F01C3; V04-V09

Alerting Abstract ...several components to connect instruction registers to receive instructions via the bus path. Instructions are **shifted** into the **instruction** registers and their validity checked. All the components containing valid instructions are set up to...

Original Publication Data by Authority

Original Abstracts:
...scan path rather than the expected register when errors are detected.
JTAG instruction signals are **shifted** **into** the scan path to determine whether an instruction error was received by a component. Data scanned into the component is **prefixed** by a header **which** is **monitored** by the JTAG **control** circuitry to detect any instruction errors. The combined data and header are padded by bits...
Claims:
...registers to receive instructions to be performed within said components via said serial bus path; **shifting** **instructions** **to** **be** performed within said components into said instruction registers; checking the validity of said instructions **shifted** **into** **said** **instruction** registers; **setting** up all of said plurality of components having instruction registers containing valid instructions to connect...

36/69,K/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006528157 - Drawing available
WPI ACC NO: 1993-337145/199342
XRPX Acc No: N1993-260536
Extracting and aligning complex variable length instructions - extracts and passes set of instruction bytes to align latch to align bytes, with aligned bytes sent to next instruction detector
Patent Assignee: SEIKO EPSON CORP (SHIH); TRANSMETA CORP (TRAN-N)
Inventor: COON B; MIYAYAMA Y; NGUYEN L T; WANG J
Patent Family (35 patents, 16 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1993020507	A2	19931014	WO 1993JP417	A	19930330	199342	B
EP 636257	A1	19950201	EP 1993906870	A	19930330	199509	E
			WO 1993JP417	A	19930330		
WO 1993020507	A3	19940106	WO 1993JP417	A	19930330	199515	E
JP 7505968	W	19950629	JP 1993517306	A	19930330	199534	E
			WO 1993JP417	A	19930330		
US 5438668	A	19950801	US 1992857599	A	19920331	199536	E
US 5546552	A	19960813	US 1992857599	A	19920331	199638	E
			US 1995440225	A	19950512		
US 5619666	A	19970408	US 1992857599	A	19920331	199720	E
			US 1995460272	A	19950602		
US 5983334	A	19991109	US 1992857599	A	19920331	199954	E
			US 1995460272	A	19950602		
			US 1997784339	A	19970116		
EP 1028370	A2	20000816	EP 1993906870	A	19930330	200040	E
			EP 2000108579	A	19930330		
JP 2000215047	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007258	A	19930330		
JP 2000215048	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007259	A	19930330		
JP 2000215049	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007260	A	19930330		
JP 2000215050	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007261	A	19930330		
JP 2000215051	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007262	A	19930330		
JP 2000215052	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007263	A	19930330		
JP 2000215053	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007264	A	19930330		
JP 2000215054	A	20000804	JP 1993517306	A	19930330	200042	E
			JP 20007265	A	19930330		
EP 636257	B1	20001108	EP 1993906870	A	19930330	200062	E
			WO 1993JP417	A	19930330		
			EP 2000108579	A	19930330		
DE 69329644	E	20001214	DE 69329644	A	19930330	200104	E
			EP 1993906870	A	19930330		
			WO 1993JP417	A	19930330		
US 6263423	B1	20010717	US 1992857599	A	19920331	200142	E
			US 1995460272	A	19950602		

			US	1997784339	A	19970116		
			US	1999401860	A	19990922		
US	20030084270	A1	20030501	US	1995460272	A	19950602	200331	E
				US	1997784339	A	19970116		
				US	1997857599	A	19970516		
				US	1999401860	A	19990922		
				US	2001852295	A	20010510		
				US	200261295	A	20020204		
KR	343530	B	20021127	WO	1993JP417	A	19930330	200334	E
				KR	1994703361	A	19940927		
KR	371929	B	20030212	WO	1993JP417	A	19930330	200341	E
				KR	1994703361	A	19940927		
				KR	2001705744	A	20010507		
JP	3544330	B2	20040721	JP	1993517306	A	20000117	200448	E
				JP	20007258	A	20000117		
JP	3544331	B2	20040721	JP	1993517306	A	20000117	200448	E
				JP	20007259	A	20000117		
JP	3544332	B2	20040721	JP	1993517306	A	20000117	200448	E
				JP	20007260	A	20000117		
JP	3544333	B2	20040721	JP	1993517306	A	20000117	200448	E
				JP	20007263	A	20000117		
JP	3544334	B2	20040721	JP	1993517306	A	20000117	200448	E
				JP	20007264	A	20000117		
JP	3544335	B2	20040721	JP	1993517306	A	20000117	200448	E
				JP	20007265	A	20000117		
JP	3547052	B2	20040728	JP	1993517306	A	19930330	200449	E
				WO	1993JP417	A	19930330		
EP	1028370	B1	20040915	EP	1993906870	A	19930330	200460	E
				EP	2000108579	A	19930330		
DE	69333630	E	20041021	DE	69333630	A	19930330	200469	E
				EP	2000108579	A	19930330		
DE	69333630	T2	20050922	DE	69333630	A	19930330	200563	E
				EP	2000108579	A	19930330		
US	6954847	B2	20051011	US	1992857599	A	19920331	200567	E
				US	1995460272	A	19950602		
				US	1997784339	A	19970116		
				US	1999401860	A	19990922		
				US	2001852295	A	20010510		
				US	200261295	A	20020204		
US	20050251653	A1	20051110	US	1992857599	A	19920331	200574	E
				US	1995460272	A	19950602		
				US	1997784339	A	19970116		
				US	1999401860	A	19990922		
				US	2001852295	A	20010510		
				US	200261295	A	20020204		
				US	2005167289	A	20050628		

Priority Applications (no., kind, date): US 2005167289 A 20050628; US 200261295 A 20020204; US 2001852295 A 20010510; US 1999401860 A 19990922; US 1997857599 A 19970516; US 1997784339 A 19970116; US 1995460272 A 19950602; US 1995440225 A 19950512; US 1992857599 A 19920331

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1993020507	A2	EN	59	17	

National Designated States,Original: JP KR

Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LU
MC NL PT SE

EP 636257	A1	EN	2	1	PCT Application WO 1993JP417 Based on OPI patent WO 1993020507
Regional Designated States,Original: DE FR GB					
WO 1993020507	A3	EN			
JP 7505968	W	JA	23	1	PCT Application WO 1993JP417 Based on OPI patent WO 1993020507
US 5438668	A	EN	40	17	
US 5546552	A	EN	44	17	Continuation of application US 1992857599 Continuation of patent US 5438668
US 5619666	A	EN	34	17	Continuation of application US 1992857599 Continuation of patent US 5438668
US 5983334	A	EN			Continuation of application US 1992857599 Continuation of application US 1995460272 Continuation of patent US 5438668 Continuation of patent US 5619666
EP 1028370	A2	EN			Division of application EP 1993906870 Division of patent EP 636257
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE					
JP 2000215047	A	JA	28		Division of application JP 1993517306
JP 2000215048	A	JA	29		Division of application JP 1993517306
JP 2000215049	A	JA	29		Division of application JP 1993517306
JP 2000215050	A	JA	29		Division of application JP 1993517306
JP 2000215051	A	JA	29		Division of application JP 1993517306
JP 2000215052	A	JA	29		Division of application JP 1993517306
JP 2000215053	A	JA	29		Division of application JP 1993517306
JP 2000215054	A	JA	29		Division of application JP 1993517306
EP 636257	B1	EN			PCT Application WO 1993JP417 Related to application EP 2000108579 Related to patent EP 1028370 Based on OPI patent WO 1993020507

Regional Designated States,Original: DE FR GB

DE 69329644	E	DE		Application EP 1993906870 PCT Application WO 1993JP417 Based on OPI patent EP 636257 Based on OPI patent WO 1993020507
US 6263423 1992857599	B1	EN		Continuation of application US Continuation of application US 1995460272 Continuation of application US 1997784339 Continuation of patent US 5438668 Continuation of patent US 5619666 Continuation of patent US 5983334
US 20030084270 1995460272	A1	EN		Continuation of application US Continuation of application US 1997784339 Continuation of application US 1997857599 Continuation of application US 1999401860 Continuation of application US 2001852295 Continuation of patent US 5619666 Continuation of patent US 5983334 Continuation of patent US 6068737 Continuation of patent US 6263423
KR 343530 95701100	B	KO		PCT Application WO 1993JP417 Previously issued patent KR Based on OPI patent WO 1993020507
KR 371929 1994703361	B	KO		PCT Application WO 1993JP417 Division of application KR Based on OPI patent WO 1993020507
JP 3544330 1993517306	B2	JA	36	Division of application JP Previously issued patent JP 2000215047
JP 3544331 1993517306	B2	JA	36	Division of application JP Previously issued patent JP 2000215048
JP 3544332 1993517306	B2	JA	36	Division of application JP Previously issued patent JP 2000215049
JP 3544333	B2	JA	36	Division of application JP

1993517306

Previously issued patent JP
2000215052

JP 3544334 B2 JA 36 Division of application JP
1993517306

Previously issued patent JP
2000215053

JP 3544335 B2 JA 37 Division of application JP
1993517306

Previously issued patent JP
2000215054

JP 3547052 B2 JA 33 PCT Application WO 1993JP417
Previously issued patent JP
07505968

Based on OPI patent WO 1993020507
EP 1028370 B1 EN Division of application EP
1993906870

Division of patent EP 636257
Regional Designated States,Original: DE FR GB
DE 69333630 E DE Application EP 2000108579
Based on OPI patent EP 1028370
DE 69333630 T2 DE Application EP 2000108579
Based on OPI patent EP 1028370
US 6954847 B2 EN Continuation of application US
1992857599

Continuation of application US
1995460272

Continuation of application US
1997784339

Continuation of application US
1999401860

Continuation of application US
2001852295

Continuation of patent US 5438668
Continuation of patent US 5619666
Continuation of patent US 5983334
Continuation of patent US 6263423
US 20050251653 A1 EN Continuation of application US
1992857599

Continuation of application US
1995460272

Continuation of application US
1997784339

Continuation of application US
1999401860

Continuation of application US
2001852295

Continuation of application US
200261295

Continuation of patent US 5438668
Continuation of patent US 5619666
Continuation of patent US 5983334
Continuation of patent US 6263423

Alerting Abstract WO A2

A portion of a stream of complex instructions is received and a set of instruction bytes is extracted starting with the first instruction bytes using an extract shifter. The set of instruction bytes are then passed to an align latch where they are aligned and output to a next instruction detector. The next instruction detector determines the end of the first instruction based on the set of instruction bytes.

An extract shifter is used to extract and provide the next set of instruction bytes to an align shifter which aligns and outputs the next instruction. The process is then repeated for the remaining instruction bytes in the stream of complex instructions.

ADVANTAGE - Allows complex instructions to run on RISC-based hardware.

Equivalent Alerting Abstract US A

The method involves receiving a portion of the stream of complex instructions and extracting a first set of instruction bytes starting with the first instruction bytes, using an extract shifter. The set of instruction bytes are then passed to an align latch where they are aligned and output to a next instruction detector. The next instruction detector determines the end of the first instruction based on the set of instruction bytes.

An extract shifter is used to extract and provide the next set of instruction bytes to an align shifter which aligns and outputs the next instruction. The process is then repeated for the remaining instruction bytes in the stream of complex instructions. The isolated complex instructions are decoded into nano-instructions which are processed by a RISC processor core.

ADVANTAGE - Provides fast operation.

Title Terms/Index Terms/Additional Words: EXTRACT; ALIGN; COMPLEX; VARIABLE ; LENGTH; INSTRUCTION; PASS; SET; BYTE; LATCH; SEND; DETECT; RISC; CISC

Class Codes

International Classification (Main): G06F-015/76, G06F-009/30, G06F-009/318 , G06F-009/32, G06F-009/38
(Additional/Secondary): G06F-009/22, G06F-009/305, G06F-009/312, G06F-009/315
US Classification, Issued: 712204000, 712209000, 712023000, 395375000, 364DIG001, 364232220, 364259700, 364259900, 395375000, 364232220, 364259700, 364259900, 395384000, 364232220, 364259700, 364259900,

395380000, 395391000, 712023000, 712041000, 712206000, 712215000, 712217000, 712209000, 712204000, 712208000, 712204000, 712023000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03; T01-F03B; T01-M04

Original Publication Data by Authority

Original Abstracts:
...instruction bytes starting with the first instruction bytes, using an
extract shifter. The set of **instruction** bytes are then passed to an align
latch where they are aligned and output to...

...the end of the first instruction based on said set of instruction bytes.
An extract **shifter** is used to extract and provide the next set of
instruction bytes to an align shifter which aligns and **outputs** the next
instruction . The process is then repeated for the remaining instruction
bytes in the stream of complex...

...set of instruction bytes. An extract shifter is used to extract and
provide the next **set** of **instruction** bytes to an align shifter which
aligns and outputs the next instruction. The process is...

...a first set of instruction bytes starting with the first instruction
bytes, using an extract **shifter** . The set **of** instruction bytes are then
passed to an align latch where they are aligned and output...

...align shifter which aligns and outputs the next instruction. The process
is then repeated for **the** remaining **instruction** bytes in the stream of
complex instructions. The isolated complex instructions are decoded into
nano...

...a first set of instruction bytes starting with the first instruction
bytes, using an extract **shifter** . **The** set of instruction bytes are then
passed to an align latch where they are aligned and output **to** a next
instruction detector. The next instruction detector determines the end of
the first instruction based on said set of instruction bytes. An extract
shifter **is** used to extract and provide the next set of instruction bytes
to an align shifter...

...to an align latch where they are aligned and output to a next
instruction detector. **The** next **instruction** detector determines the end

of the first instruction based on said set of instruction bytes. An extract
shifter is **used** to extract and provide the next set of instruction bytes to an align shifter which...

...process is then repeated for the remaining instruction bytes in the stream of complex instructions. **The** isolated complex **instructions** are
decoded into nano-instructions which are processed by a RISC processor core
...

...a first set of instruction bytes starting with the first instruction bytes, using an extract **shifter** . The set of instruction bytes are then
passed to an align latch where they are...

...is used to extract and provide the next set of instruction bytes to an
align **shifter** which aligns **and** outputs the next instruction. The process is then repeated **for** the remaining **instruction** bytes in the stream of complex instructions. The isolated complex instructions are **decoded** into nano- **instructions** which are processed by a RISC processor
core...

...to a next instruction detector. The next instruction detector determines
the end of the first **instruction** based on said set of instruction bytes.
An extract shifter is used to extract and provide the next set of instruction bytes to an align **shifter** which aligns and outputs the next
instruction. The process is then repeated for the remaining...

...a first set of instruction bytes starting with the first instruction bytes, using an extract **shifter** . The **set** of instruction bytes are then
passed to an align latch where they are aligned and...

...The next instruction detector determines the end of the first instruction based on said set **of** **instruction** bytes. An extract shifter
is used to extract and provide the next set of instruction bytes to an align **shifter** **which** aligns and outputs the next instruction. The process is then repeated for the remaining instruction bytes in the stream
of complex **instructions** . The isolated complex instructions are decoded
into nano-instructions which are processed by a RISC...

...a first set of instruction bytes starting with the first instruction bytes, using an extract **shifter** . The set **of** instruction bytes are then
passed to an align latch where they are aligned and output...

...next instruction detector determines the end of the first

instruction
based on said set of **instruction** bytes. An extract **shifter** is used to
extract and provide the next set of instruction bytes to an align **shifter**
which **aligns** and outputs the next instruction. The process is then
repeated for the remaining instruction bytes in the stream of complex
instructions. **The** isolated complex **instructions** are decoded into
nano-instructions which are processed by a RISC processor core...a first
set of instruction bytes starting with the first instruction bytes, using
an extract **shifter** . The set **of** instruction bytes are then passed to an
align latch where they are aligned and output...

...a first set of instruction bytes starting with the first instruction
bytes, using an extract **shifter** . The set of instruction bytes are then
passed to an align latch where they are...

...the end of the first instruction based on said set of instruction bytes.
An extract **shifter** is used to extract and provide the next set of
instruction bytes to an align...
Claims:
A superscalar microprocessor for executing instructions obtained from an
instruction store, said microprocessor comprising:a **fetch circuit** to
fetch a plurality of **CISC** instructions from said instruction store,
the plurality of CISC instructions being in program order;a...

...by said decoder into one or more first RISC instructions and one or more
second **RISC instructions** , **respectively** , per clock
cycle,</br>wherein
said execution unit further comprises first and second registers each
comprising...

...means into one or more first RISC instructions and one or more second
RISC instructions, **respectively** , per clock **cycle**
,</br>characterised
by</br> **means** for storing data in a plurality of registers
identifiable by register references, said plurality of...set of instruction
bytes is extracted starting with the first instruction bytes using an
extract **shifter** . The set **of** instruction bytes are then passed to an
align latch where they are aligned and output...a first set of instruction
bytes starting with the first instruction bytes, using an extract **shifter**
; (3) passing **said** set of instruction bytes to an align latch; (4)
outputting the aligned instruction bytes from...
...the contents of said first and second instruction latches into a

final
instruction bucket on a nano- instruction -by-nano-instruction basis, wherein said combining comprises storing said first instruction latch nano-instruction...A superscalar microprocessor for executing instructions
obtained from an instruction store, said microprocessor comprising:a fetch
circuit to fetch a plurality of CISC instructions from said instruction store, the plurality of CISC instructions being...

...instruction storage locations, wherein said first RISC instructions and
said second RISC instructions are stored in said first register .

36/69,K/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005601609 - Drawing available
WPI ACC NO: 1991-209693/199129
XRPX Acc No: N1991-160078
Data processing system with instruction tag - has processor tagging memory to register instructions while pipelined execution of arithmetic instructions continues
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: HICKS T N; MYHONG N; NGUYENPHU M
Patent Family (10 patents, 6 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 437044	A	19910717	EP 1990313353	A	19901207	199129	B
AU 199066753	A	19910627				199133	E
CN 1052740	A	19910703				199215	E
US 5150470	A	19920922	US 1989453529	A	19891220	199241	E
NZ 236142	A	19921223	NZ 236142	A	19901120	199308	E
AU 639953	B	19930812	AU 199066753	A	19901120	199339	E
EP 437044	A3	19921104	EP 1990313353	A	19901207	199342	E
KR 199308035	B1	19930825	KR 199020196	A	19901208	199432	E
EP 437044	B1	19950222	EP 1990313353	A	19901207	199512	E
DE 69017178	E	19950330	DE 69017178	A	19901207	199518	E
			EP 1990313353	A	19901207		

Priority Applications (no., kind, date): US 1989453529 A 19891220

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 437044	A	EN			
Regional Designated States,Original: DE FR GB					
US 5150470	A	EN	14	8	
NZ 236142	A	EN			
AU 639953	B	EN			Previously issued patent AU 9066753
EP 437044	A3	EN			
EP 437044	B1	EN	15		
Regional Designated States,Original: DE FR GB					
DE 69017178	E	DE			Application EP 1990313353 Based on OPI patent EP 437044

Alerting Abstract EP A

A multiprocessing system has a floating point processor (16) executing arithmetic instructions, and a fixed point processor (14) executing load instructions. Register to register and register to memory instructions are placed in a queue, and memory to register instructions are placed in a second (load) queue.

When a floating point arithmetic instruction requires data that is being loaded as a result of a load instruction, the floating point arithmetic

instruction is tagged in its queue. When an instruction receives its data,
it is provided to the floating point processor for execution.
ADVANTAGE - Reduces delays caused by fetching information from memory.
@(14pp Dwg.No.1/8)@

Equivalent Alerting Abstract US A
The data processing system has an instruction execution circuit that executes a first type of instruction. Also includes is a **fetch circuit**
that **fetches** instructions from a memory and fetches data from the memory
in response to a second type of instruction. An instruction decoder is included that decodes fetched instructions and dispatches instructions of
the first type to an instructions queueing circuit. The instruction decoder
further dispatches instructions of the second type to the **fetching circuit** .
The instruction queueing circuit includes the capability to store decoded
instructions of the first type while tagging these instructions when data
required for the execution of these instructions has not been fetched. The
instruction queueing circuit further clears these tags of these instructions of the first type when data that is required for the execution
has been fetched. The instruction queueing circuit serially provides the
untagged instructions of the first type to the instruction execution circuit.
ADVANTAGE - Has tags indicating outstanding data status.

Title Terms/Index Terms/Additional Words: DATA; PROCESS; SYSTEM; INSTRUCTION; TAG; PROCESSOR; MEMORY; REGISTER; PIPE; EXECUTE; ARITHMETIC;
CONTINUE

Class Codes
International Classification (Main): G06F-009/38
International Classification (+ Attributes)
IPC + Level Value Position Status Version
G06F-0015/16 A I L R 20060101
G06F-0009/38 A I R 20060101
G06F-0015/16 C I L R 20060101
G06F-0009/38 C I R 20060101
US Classification, Issued: 395375000, 364DIG001, 364239400, 364258400, 364262800

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B

Equivalent Alerting Abstract ...an instruction execution circuit that executes a first type of instruction. Also includes is a **fetch**

circuit
that **fetches** instructions from a memory and fetches data from the memory
in response to a second...

...instructions queueing circuit. The instruction decoder further dispatches instructions of the second type to the **fetching circuit** .

Original Publication Data by Authority

Original Abstracts:
...instruction execution circuit 16 that executes a first type of instruction. Also included is a **fetch circuit** that **fetches** instructions from a memory 10 and fetches data from the memory in response
to a...

...instruction queueing circuit. The instruction decoder further dispatches
instructions of the second type to the **fetching circuit** . The instruction queueing circuit includes the capability to store decoded instructions of the first type...

...an instruction execution circuit that executes a first type of instruction. Also included is a **fetch circuit** that **fetches** instructions from a memory and fetches data from the memory in response to
a second...

...instruction queueing circuit. The instruction decoder further dispatches
instructions of the second type to the **fetching circuit** . The instruction queueing circuit includes the capability to store decoded instructions of the first type...
Claims:
...are queued before execution, characterised in that the system includes
decoding means 26, 28 to **decode** the **instructions** and to **separate** arithmetic instructions into a first queue in the buffering means and load
instructions into a...

...tag control means (68), characterised in that the system includes decoding means (26, 28) to **decode** the **instructions** and to **separate** arithmetic instructions into a first queue in the buffering means and load
instructions into a...

36/69,K/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0004838112 - Drawing available
WPI ACC NO: 1989-214204/198930
Pipelined processor for CPU or microprocessor in computer system - computes effective branch destination address of conditional branch instruction before or in parallel with execution of instruction
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: USAMI K
Patent Family (5 patents, 6 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
EP 324952	A	19890726	EP 1988121006	A	19881215	198930	B
US 5237664	A	19930817	US 1988272948	A	19881118	199334	E
KR 199209999	B1	19921110	KR 1989482	A	19890118	199413	E
EP 324952	B1	19961023	EP 1988121006	A	19881215	199647	E
DE 3855629	G	19961128	DE 3855629	A	19881215	199702	E
			EP 1988121006	A	19881215		

Priority Applications (no., kind, date): JP 19887035 A 19880118

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 324952	A	EN	11	7	
Regional Designated States,Original: DE FR GB IT					
US 5237664	A	EN	9	7	
EP 324952	B1	EN	12	7	
Regional Designated States,Original: DE FR GB IT					
DE 3855629	G	DE			Application EP 1988121006 Based on OPI patent EP 324952

Alerting Abstract EP A

The information processing system comprises a storage (3, 7) for fetching and storing instructions to be executed and a decoder (8) for an instruction supplied from the storage (3, 7). The decoder sends an effective address generating request according to a result of the decoding.

An effective address computer receives the request from the decoder (8) to compute an effective address of the decoded instruction. If the decoded instruction is a conditional branch instruction, a destination address of the conditional branch instruction is computed to prefetch an instruction located at the branch destination address at least before the conditional branch instruction is completely executed (10).

ADVANTAGE - Improves performance of CPU without increasing hardware.

Equivalent Alerting Abstract US A

The pipeline **circuit** includes instruction **fetching** unit to fetch instruction from memory at an address **specified** by program counter,

instruction decoder for **decoding instruction** code from instruction
fetching unit, sending an effective address generating request and information related to addressing mode to an effective address generating
unit instruction execution unit

A pipeline circuit adopted for CPU or a microprocessor in a computer system, computes the effective branch destination address of a conditional
branch instruction before or in parallel with the execution of the conditional branch instruction. According to result of execution of instruction just before the conditional branch instruction is met, it is
judged and if the branch condition is met, it executes the conditional branch instruction while prefetching and decoding an instruction located at
the branch destination address.

USE/ADVANTAGE - For CPU or microprocessor, capable of improving performance of CPU without drastically increasing amount of hardware and
without complicating controls.

Title Terms/Index Terms/Additional Words: PIPE; PROCESSOR; CPU; MICROPROCESSOR; COMPUTER; SYSTEM; COMPUTATION; EFFECT; BRANCH; DESTINATION; ADDRESS; CONDITION; INSTRUCTION; PARALLEL; EXECUTE

Class Codes

International Classification (Main): G06F-009/38
International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
G06F-0009/32	A	I L	R	20060101
G06F-0009/38	A	I	R	20060101
G06F-0009/32	C	I L	R	20060101
G06F-0009/38	C	I	R	20060101

US Classification, Issued: 395375000, 364DIG001, 364231800, 364261300, 364261500, 364262400, 364263000, 364263100, 364263200

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03B

Equivalent Alerting Abstract ...The pipeline **circuit** includes instruction **fetching** unit to fetch instruction from memory at an address
specified by program counter, **instruction decoder** for **decoding instruction** code from instruction fetching unit, sending an effective address generating request and information related to...

? t 36/9/16-17

36/9/16 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03689538 **Image available**
ELECTRONIC COMPUTER

PUB. NO.: 04-054638 [JP 4054638 A]

PUBLISHED: February 21, 1992 (19920221)
INVENTOR(s): MINAGAWA KENJI
AIKAWA TAKESHI
SAITO MITSUO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 02-164552 [JP 90164552]
FILED: June 22, 1990 (19900622)
INTL CLASS: [5] G06F-009/38; G06F-009/38
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1365, Vol. 16, No. 247, Pg. 25, June
05, 1992 (19920605)

ABSTRACT

PURPOSE: To efficiently execute the parallel processing of plural instructions by decoding directly plural instructions fetched by a **fetching circuit** in a first processing unit and detecting the execution sequence dependency between plural instructions.

CONSTITUTION: Four instructions fetched in an instruction buffer 1 are distributed and supplied to plural instruction execution units 3 (3a, 3b - 3n), respectively in accordance with the classification of its instruction through an instruction distributor 2. These respective instruction executing units 3 are provided with a decoder 4, **respectively , decode** an **instruction** distributed and supplied selectively from the instruction buffer 1 under the control of the distributor 2, respectively, access a register in accordance with data of a register field shown by a result of its decoding and execute its instruction. In such a way, it is possible to execute the processing of a simultaneous execution possibility decision within a processing time of a decoding stage without setting newly the processing time required for a decision of simultaneous execution possibility between the instructions.

36/9/17 (Item 2 from file: 347)

01906111 **Image available**

ACCURACY MONITOR METHOD OF SAMPLING CYCLE

PUB. NO.: 61-120211 [JP 61120211 A]
PUBLISHED: June 07, 1986 (19860607)
INVENTOR(s): TSUKUDA HISASHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-242767 [JP 84242767]
FILED: November 16, 1984 (19841116)
INTL CLASS: [4] G05B-021/00; G06F-003/05; G11C-027/02
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation); 45.2 (INFORMATION PROCESSING -- Memory Units); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R005 (PIEZOELECTRIC FERROELECTRIC SUBSTANCES)
JOURNAL: Section: P, Section No. 507, Vol. 10, No. 305, Pg. 145, October 17, 1986 (19861017)

ABSTRACT

PURPOSE: To monitor the presence or absence of a fault with high accuracy by measuring the width of a sampling cycle by the time decided by the executing time and frequency of an instruction word of a program and comparing the measured value with a standard for decision.

CONSTITUTION: A **circuit** device which **fetches** the input information by sampling consists of a crystal oscillation circuit 1 which produces the master clock signal, a dividing circuit 2 which divides the master clock signal to produce the sample signal, a sample holding **circuit** 3 which **fetches** the analog input information synchronously with the sample signal, an A/D converting circuit 4, a memory 5 and a primary arithmetic unit 6. Then a specific program for monitor of sampling cycle accuracy is stored to a memory of the unit 6. This action is repeated by making use of the processing idle time. The specific program includes an increment instruction, a cycle **shift** deciding **instruction** and a branching instruction with repeats both said increment and deciding instructions. Then the program is measured by the time decided by the executing time of an instruction word. This measured value is compared with the upper and lower limit levels of the deciding standard. Thus the presence or absence

of a fault can be monitored with high accuracy.
?